

PWWAA

LC Marseille

LA-6842P REV 0.2 Schematic

Intel Processor (ARD) /PCH (HM55)

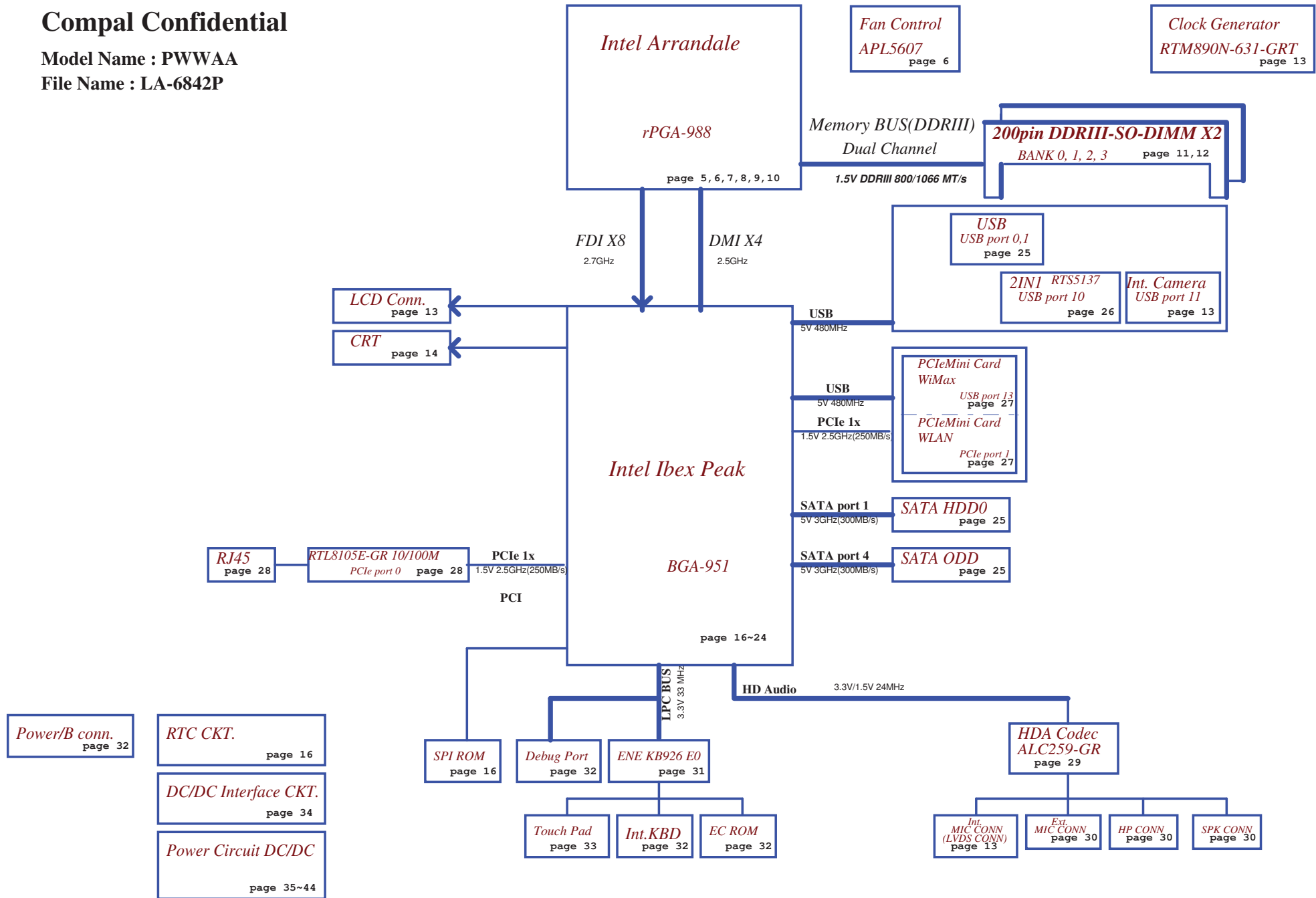
2010-07-22 Rev 0.2

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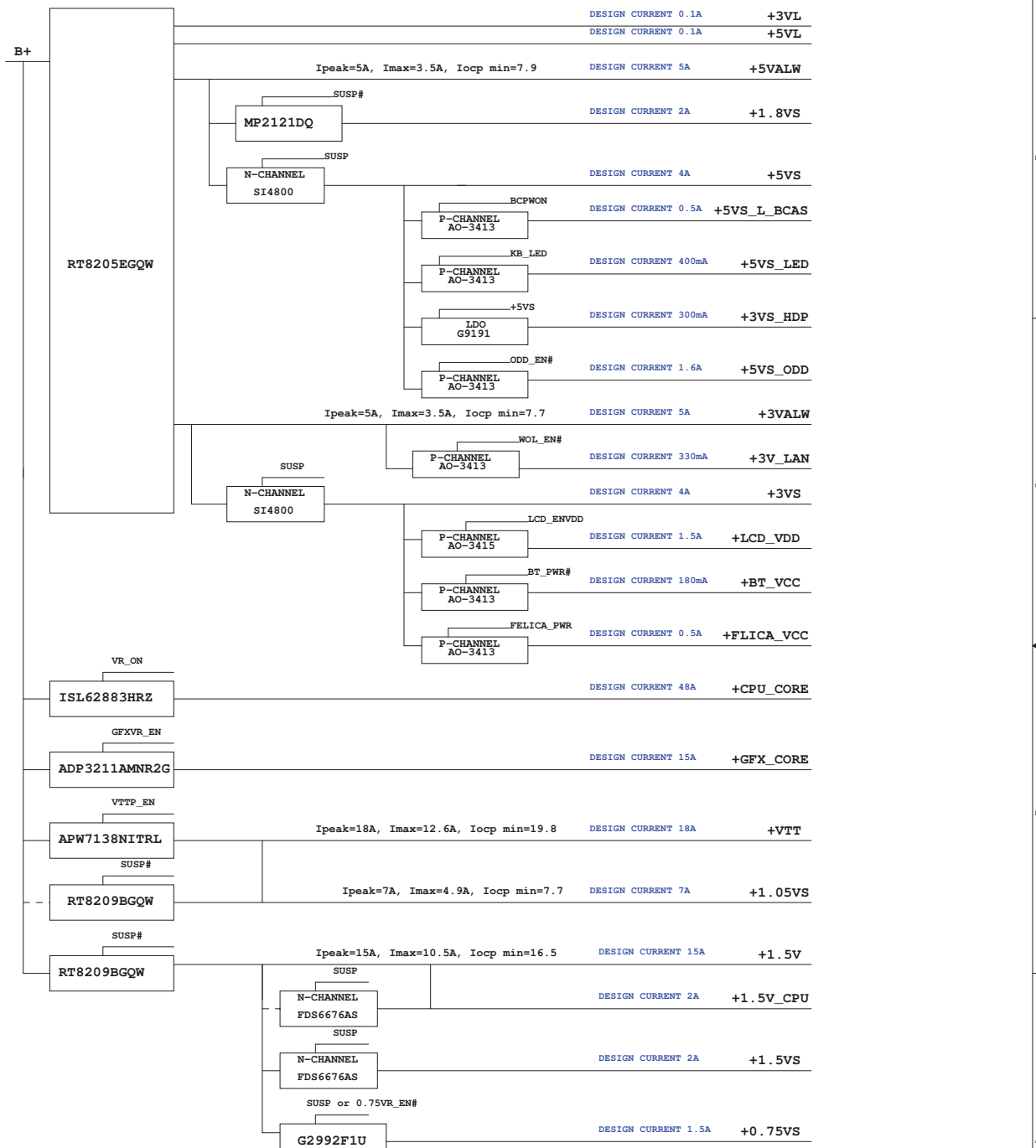
Compal Confidential

Model Name : PWWAA

File Name : LA-6842P



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Voltage Rails (O MEANS ON X MEANS OFF)

<div> <div>power plane</div> <div>State</div> </div>	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
Power	Device	HEX	Address				

BTO Option Table

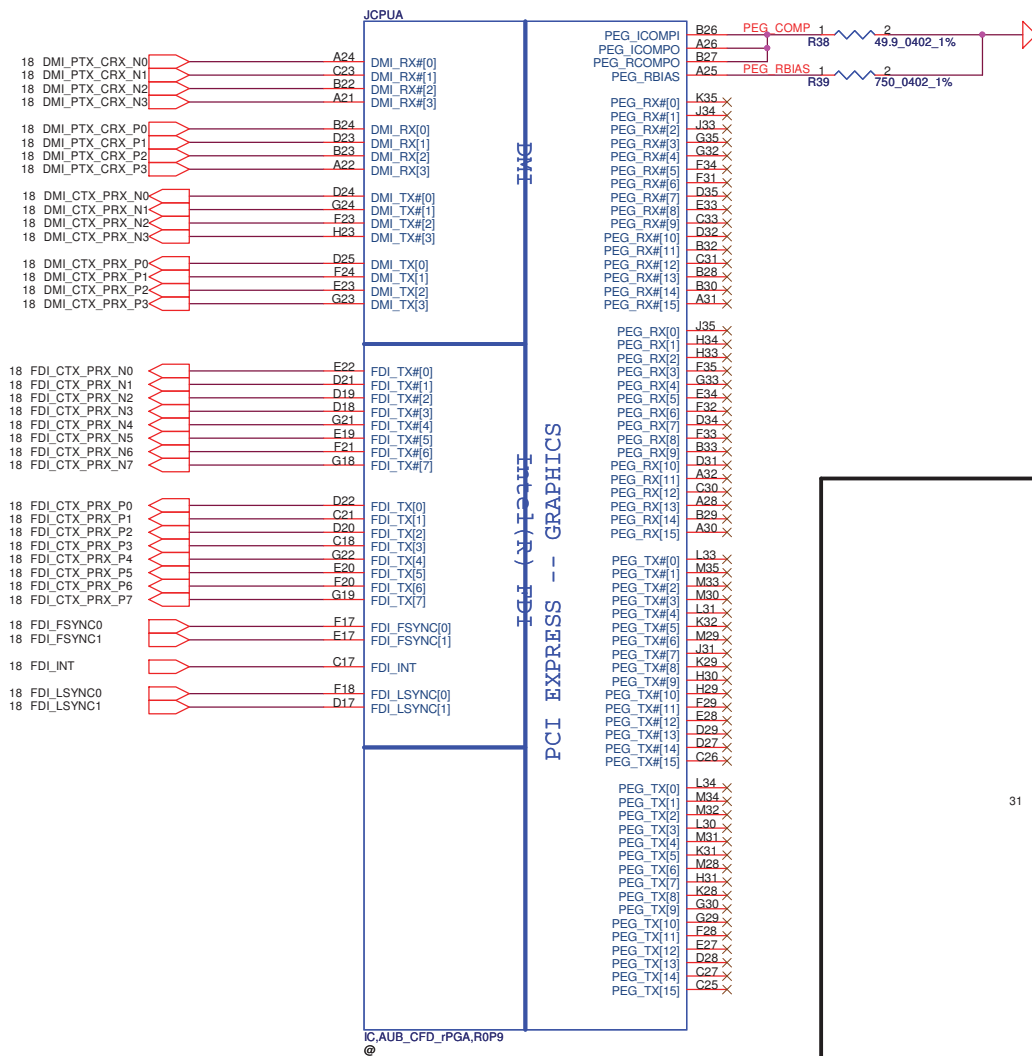
Function	MINI PCI-E SLOT		LAN					
description			SLOT1	LAN				
explain			WLAN/BT	10/100M				
BTO								

Function				Camera & Mic		
description				Camera & Mic		
explain				Camera & Mic		
BTO				CAM@		

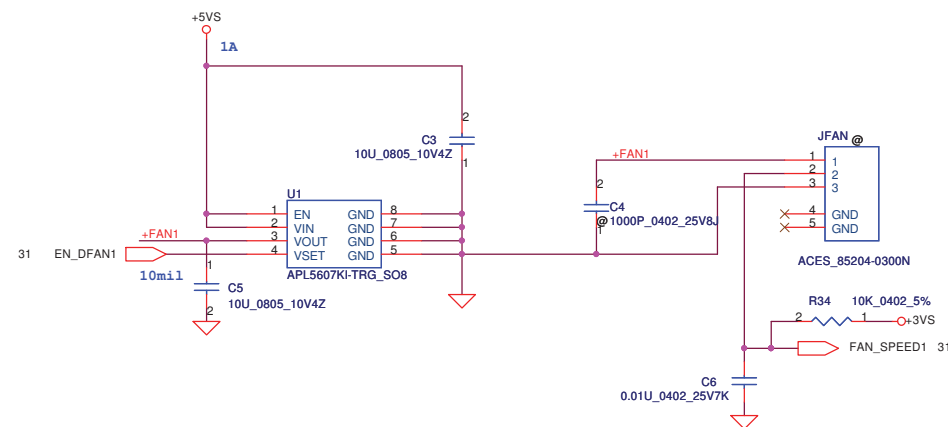
Function	S3 Power Saving	
description	S3 Power Saving	
explain		Power Saving
BTO		

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

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				Size	Document Number	Rev
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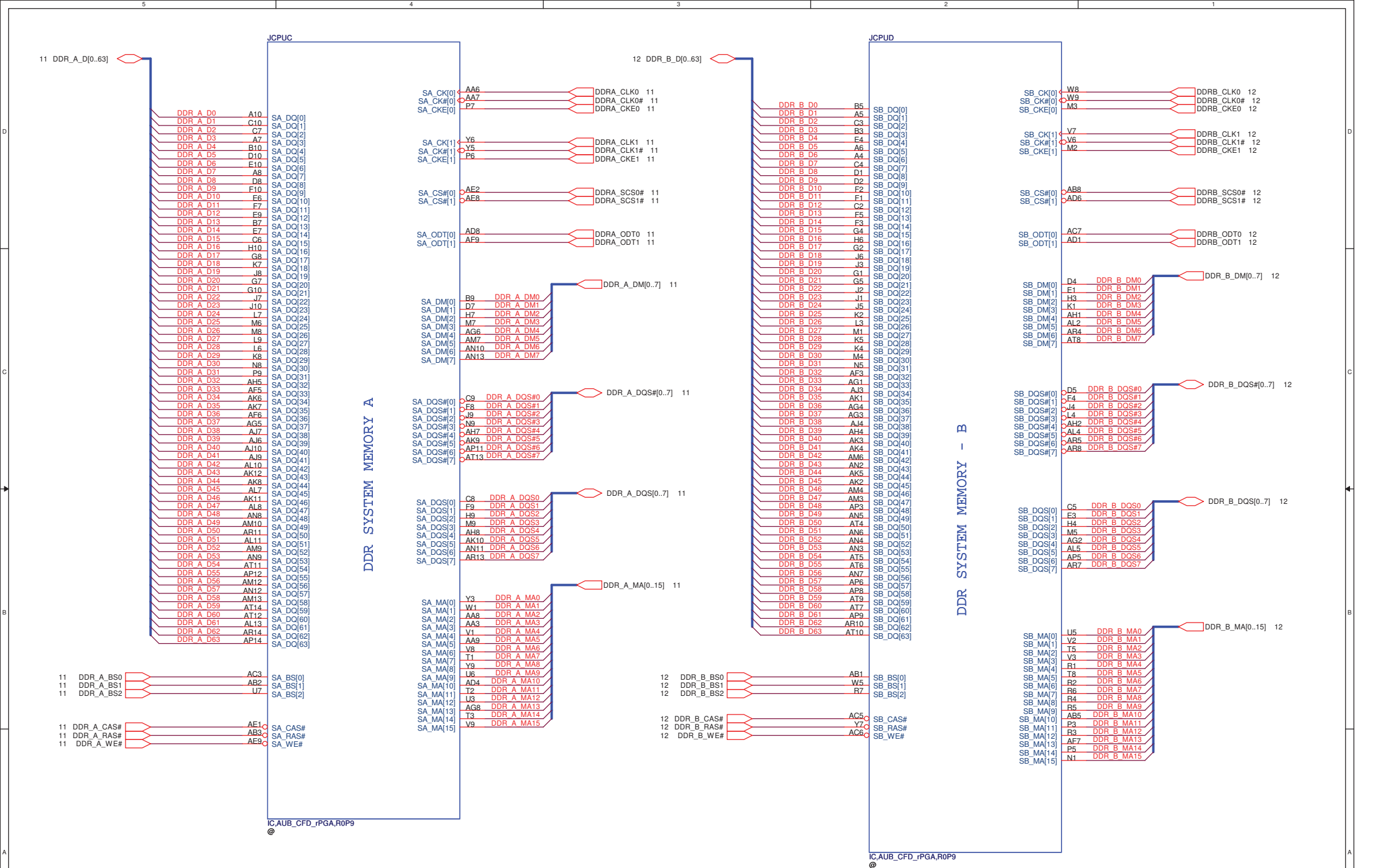
FAN Control Circuit



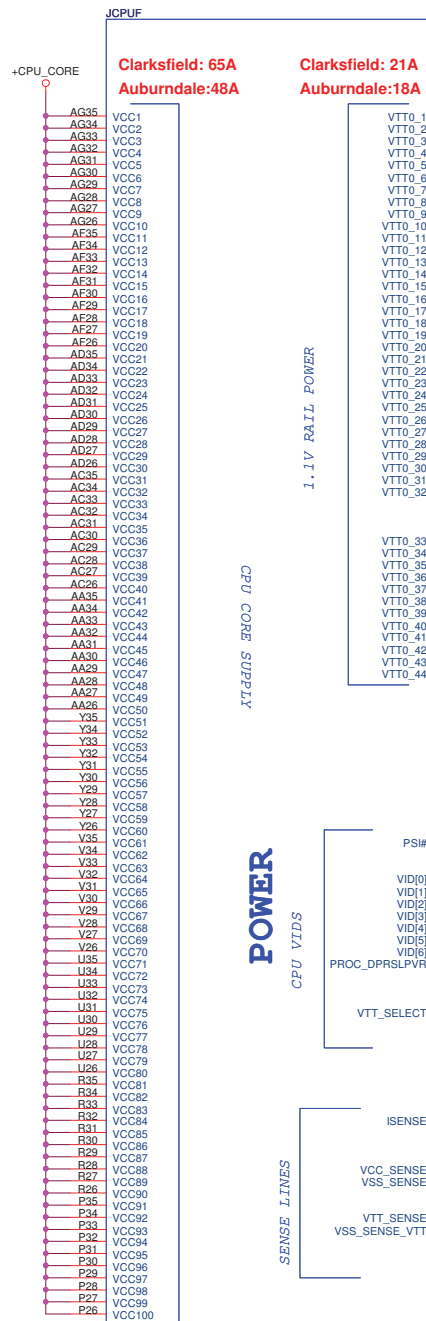
Remove Cap, for EMI

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										CPU DMI/FDI/PEG	
										PWWAA LA6842P M/B	
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Material Note (+VTT):
390uF/ 10mohm, number are 3,
power x1, HW x2

(Place these capacitors under CPU socket Edge, top layer)

Power team request for F-Din

CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V

(Place these capacitors between inductor and socket on Bottom)

(Place these capacitors under CPU socket, top layer)

(Place these capacitors on CPU cavity, Bottom Layer)

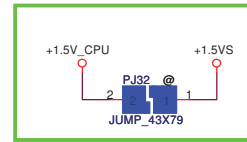
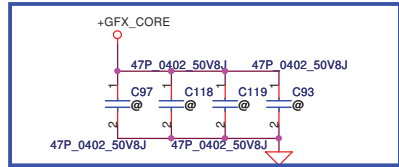
TOP side (under inductor)

Check list:

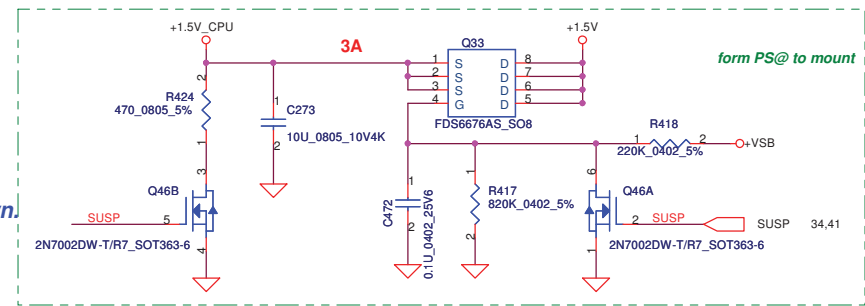
+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

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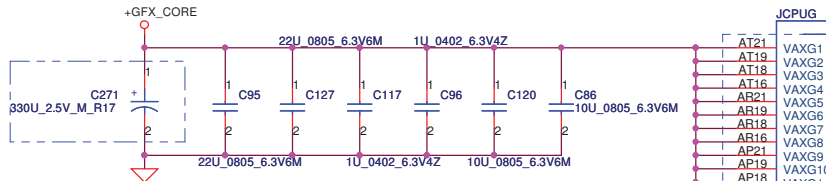
For EMI request



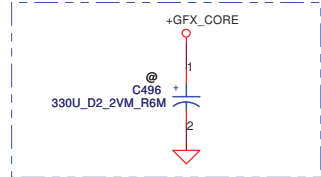
7/22 modified for cost down



Change C271 to 4.5mm height OS-CON at PVT

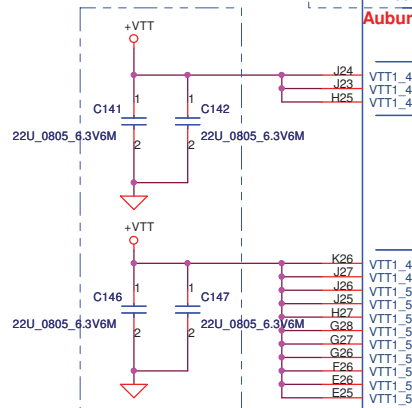


Add C496 Co-Layout with C271



For POLY Cap.

0714 --> C271 mount, C496 unmount



(Place these capacitors under CPU socket, top layer)

JCPUG

- AT21 VAXG1
- AT19 VAXG2
- AT18 VAXG3
- AT16 VAXG4
- AR21 VAXG5
- AR19 VAXG6
- AR18 VAXG7
- AR16 VAXG8
- AP21 VAXG9
- AP19 VAXG10
- AP18 VAXG11
- AP16 VAXG12
- AN21 VAXG13
- AN19 VAXG14
- AN18 VAXG15
- AN16 VAXG16
- AM21 VAXG17
- AM19 VAXG18
- AM18 VAXG19
- AM16 VAXG20
- AL21 VAXG21
- AL19 VAXG22
- AL18 VAXG23
- AK21 VAXG24
- AK19 VAXG25
- AK18 VAXG26
- AK16 VAXG27
- AJ21 VAXG28
- AJ19 VAXG29
- AJ18 VAXG30
- AJ16 VAXG31
- AH21 VAXG32
- AH19 VAXG33
- AH18 VAXG34
- AH16 VAXG35
- AH14 VAXG36

Auburndale:22A

Clarkfield: 5A

Auburndale:3A

Clarkfield: 21A

Auburndale:18A

Clarkfield: 0.6A

Auburndale:1.35A

Clarkfield: 0.6A

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Auburndale:1.35A

GRAPHICS

POWER

FDI

PEG & DM1

Clarkfield: 0.6A

Auburndale:1.35A

Clarkfield: 0.6A

Auburndale:1.35A

Clarkfield: 0.6A

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Auburndale:1.35A

SENSE LINES

DDR3 - 1.5V RAILS

1.1V

1.8V

Clarkfield: 0.6A

Auburndale:1.35A

Clarkfield: 0.6A

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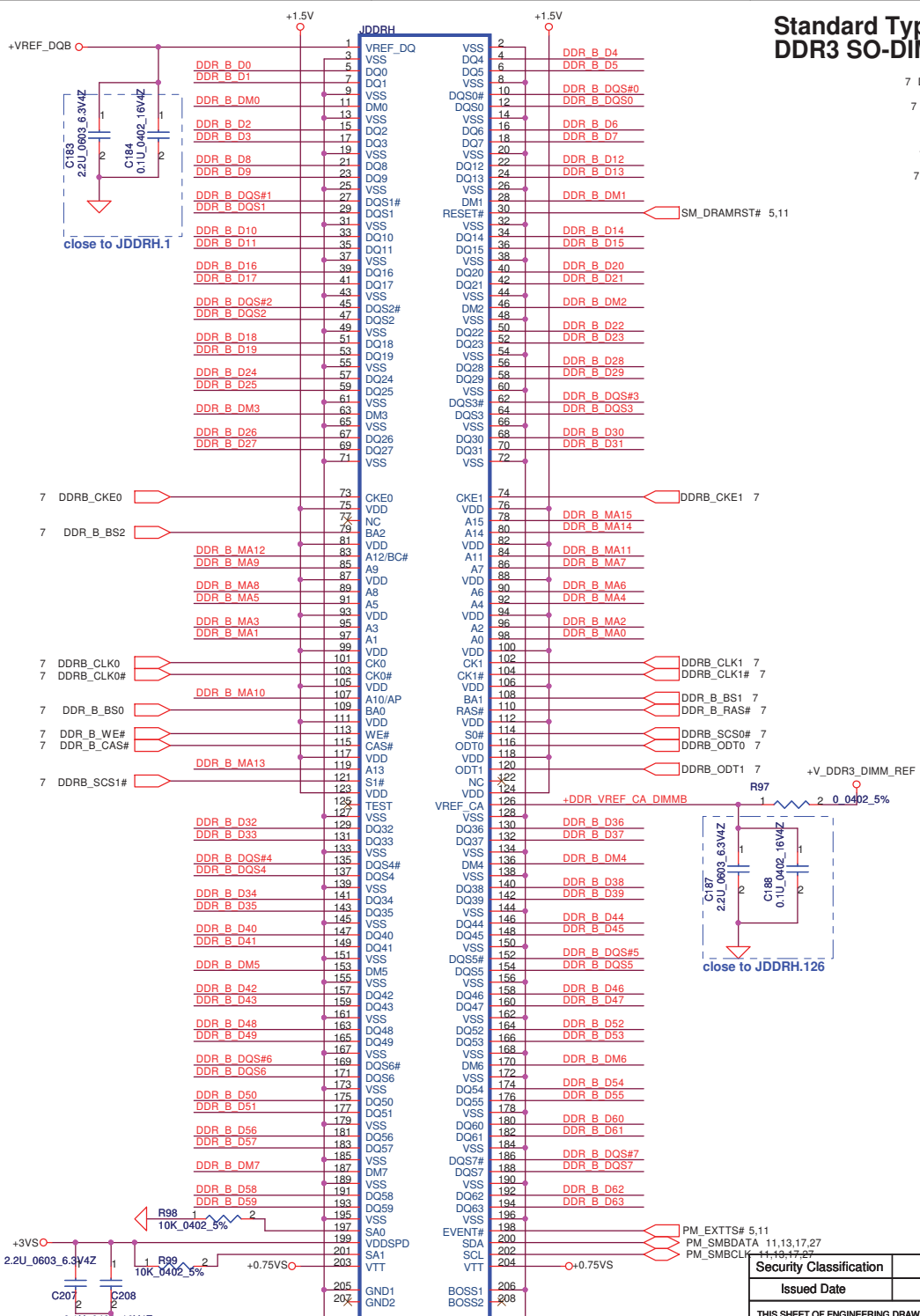
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Clarkfield: 0.6A

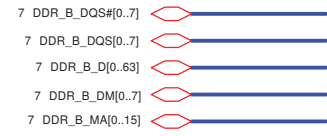
Auburndale:1.35A

Clarkfield: 0.6A

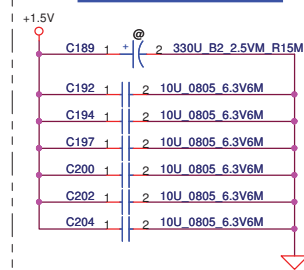




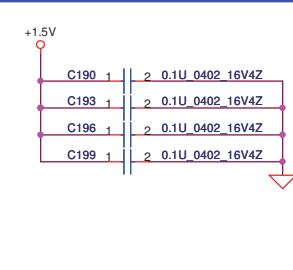
Standard Type DDR3 SO-DIMM B



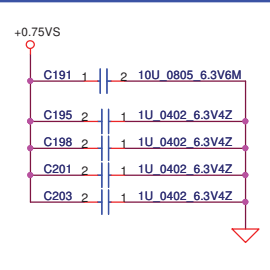
Layout Note:
Place near JDDRRH



Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

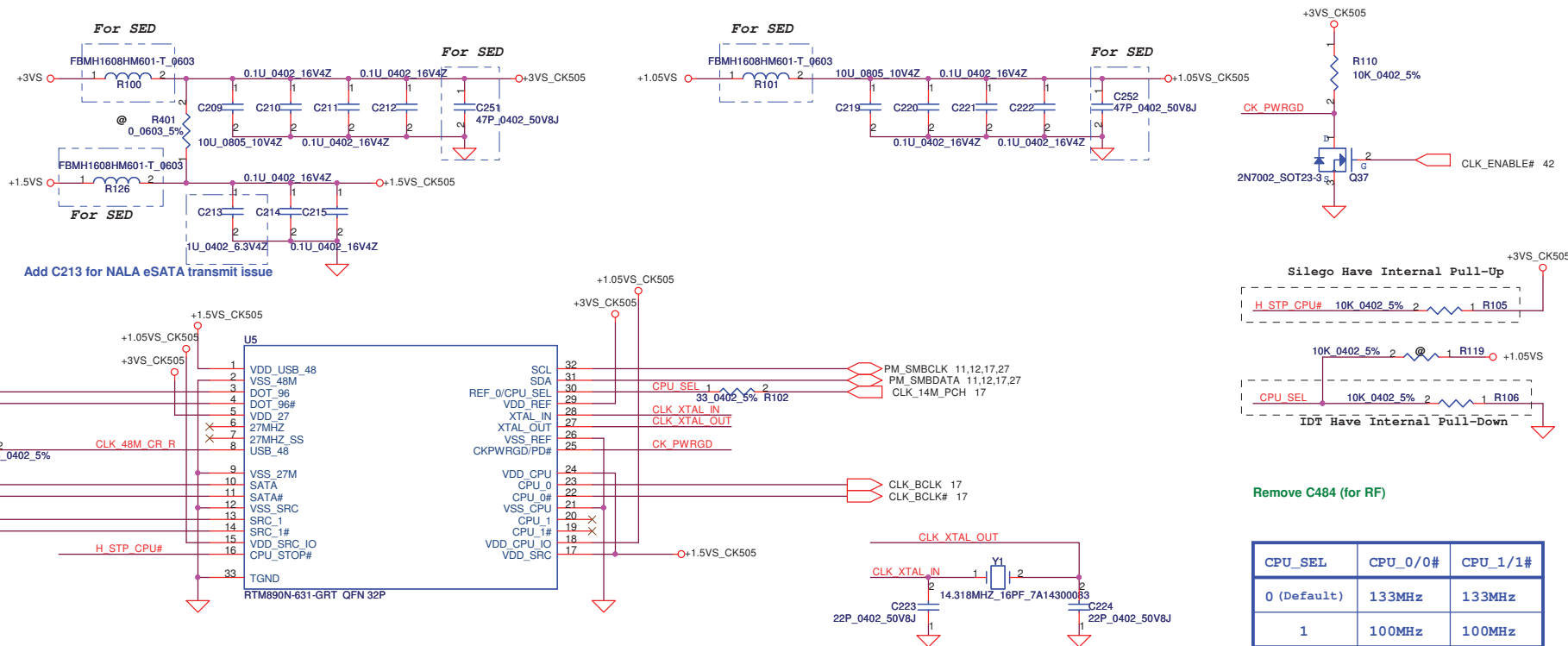


Layout Note:
Place near JDDRRH.203 and 204

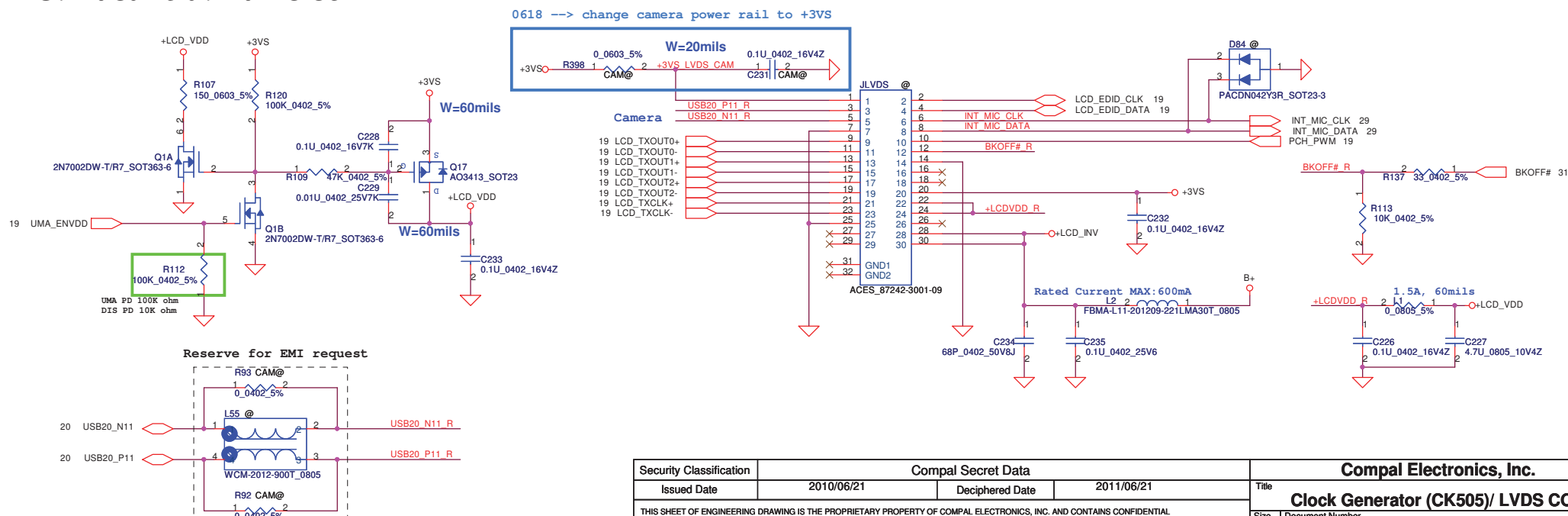


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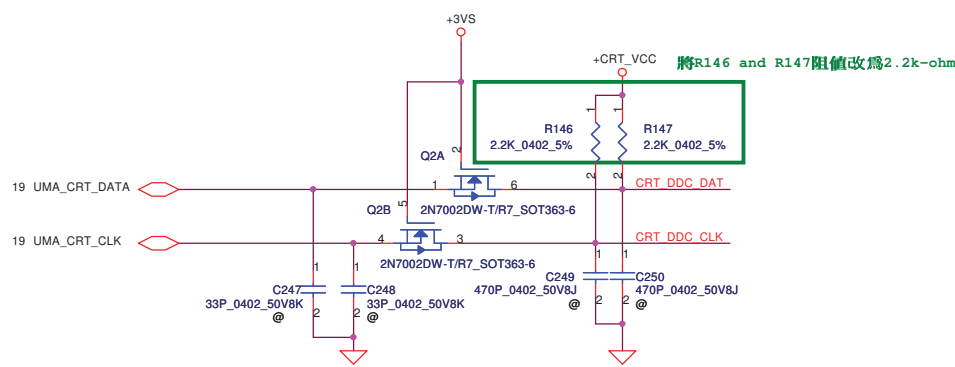
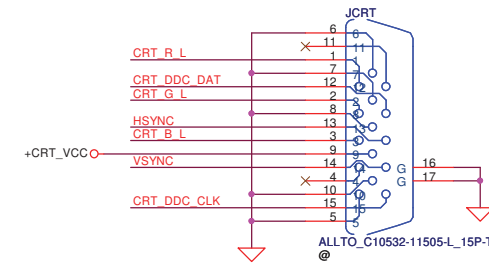
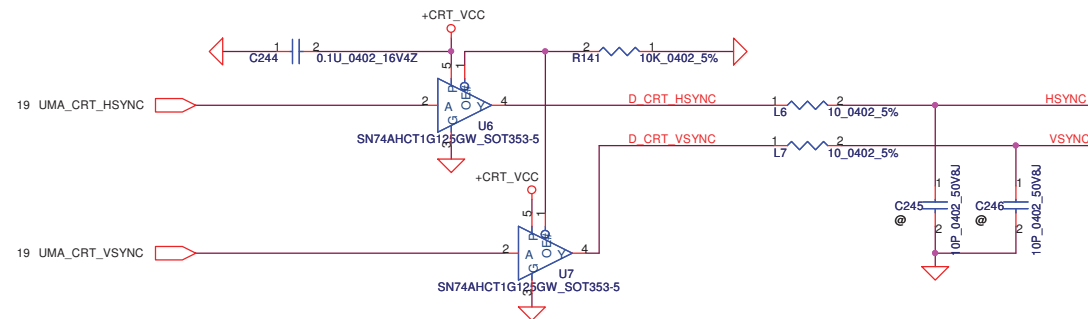
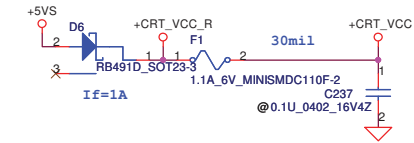
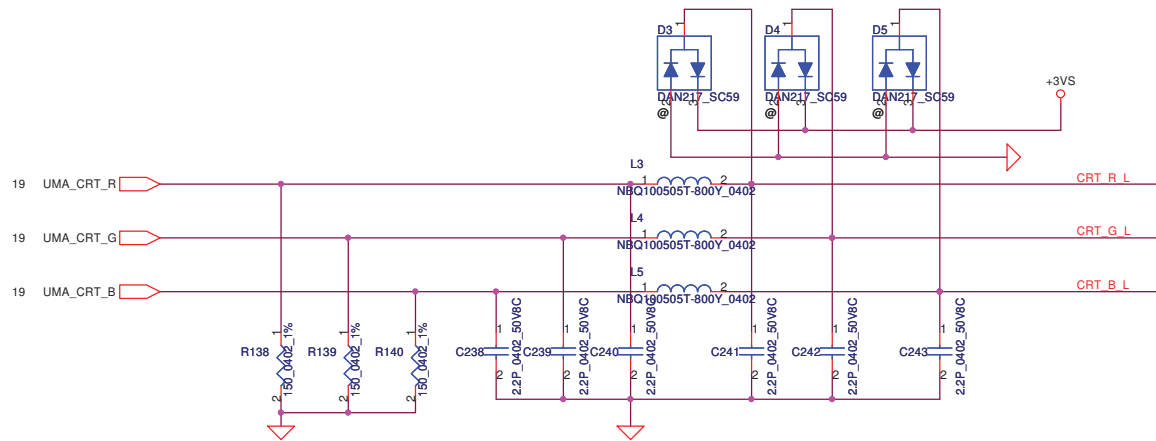
Clock Generator



LVDS / Int.Camera / Int.MIC Conn



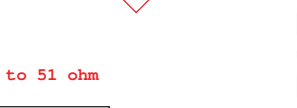
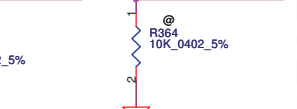
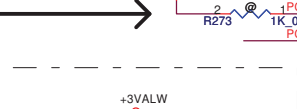
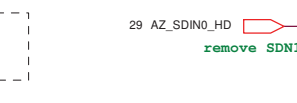
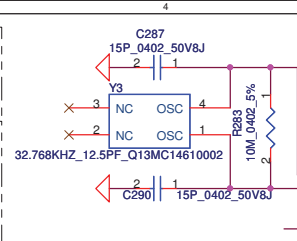
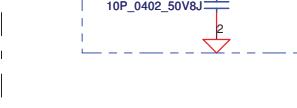
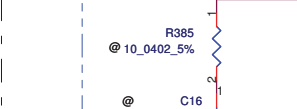
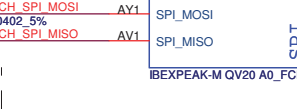
CRT CONNECTOR



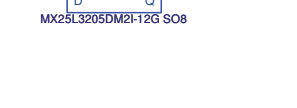
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Size	Document Number	Rev		PWWAA LA6842P M/B	
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0624 --> Remove BIOS ROM Debug Circuit

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				Rev	0.2

[illegible]

Security Classification	
Issued Date	
THIS SHEET OF ENGINEERING DRAWING IS:	



Model	Compal Electronics
Model	PCH-SPI/SATA/LPC/

For LAN

For WLAN

28 PCIE_PRX_C_LANTX_N1
28 PCIE_PRX_C_LANTX_P1
28 PCIE_PT_X_C_LANRX_N1
28 PCIE_PT_X_C_LANRX_P1

27 PCIE_PRX_WLANTX_N2
27 PCIE_PRX_WLANTX_P2
27 PCIE_PT_X_C_WLANRX_N2
27 PCIE_PT_X_C_WLANRX_P2

remove NewCard PCIE

remove JET PCIE

remove CardReader PCIE

LAN

WLAN

28 CLK_LAN#
28 CLK_LAN
28 CLKREQ_LAN#
27 CLK_WLAN#
27 CLK_WLAN
27 CLKREQ_WLAN#

form CLKREQ_NEW# to PCH_GPIO20

form CLKREQ_WLAN# to PCH_GPIO25

form CLKREQ_JET# to PCH_GPIO25

form CLKREQ_CR# to PCH_GPIO26

remove NEWCARD CLK

remove JET CLK

PCH_GPIO20

PCH_GPIO25

PCH_GPIO26

PCH_GPIO44

PCH_GPIO45

PCH_GPIO56

U11B

PCIE_PRX_C_LANTX_N1
PCIE_PRX_C_LANTX_P1
PCIE_PT_X_C_LANRX_N1
PCIE_PT_X_C_LANRX_P1

PCIE_PRX_WLANTX_N2
PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCIE_PT_X_C_WLANRX_N2
PCIE_PT_X_C_WLANRX_P2

PCI-E*

Controller Link

PEG

From CLK BUFFER

Clock Flex

SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75

CL_CLK1
CL_DATA1
CL_RST1#

PEG_A_CLKRQ# / GPIO47
CLKREQ_PEG#

CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_BCLK_N
CLKIN_BCLK_P

CLKIN_DOT_96N
CLKIN_DOT_96P

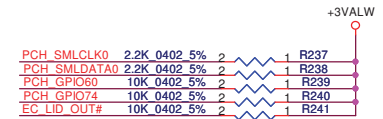
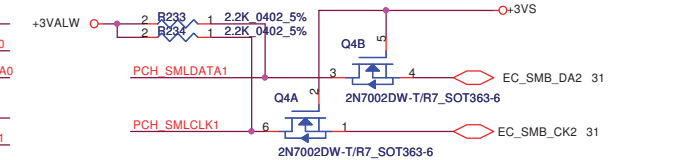
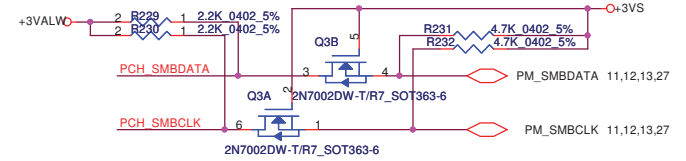
CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P

REFCLK14IN
CLKIN_PCIELOOPBACK

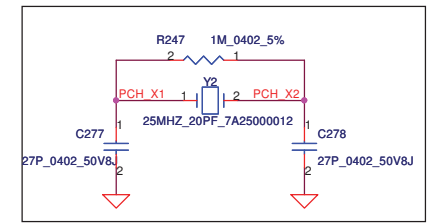
XTAL25_IN
XTAL25_OUT

XCLK_RCOMP

CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67

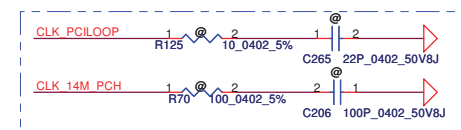


FROM CLK GEN FOR: 133/100/96/14.318 MHZ

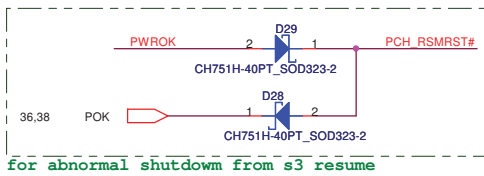
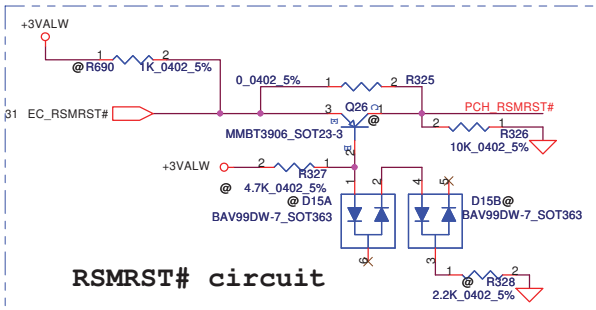
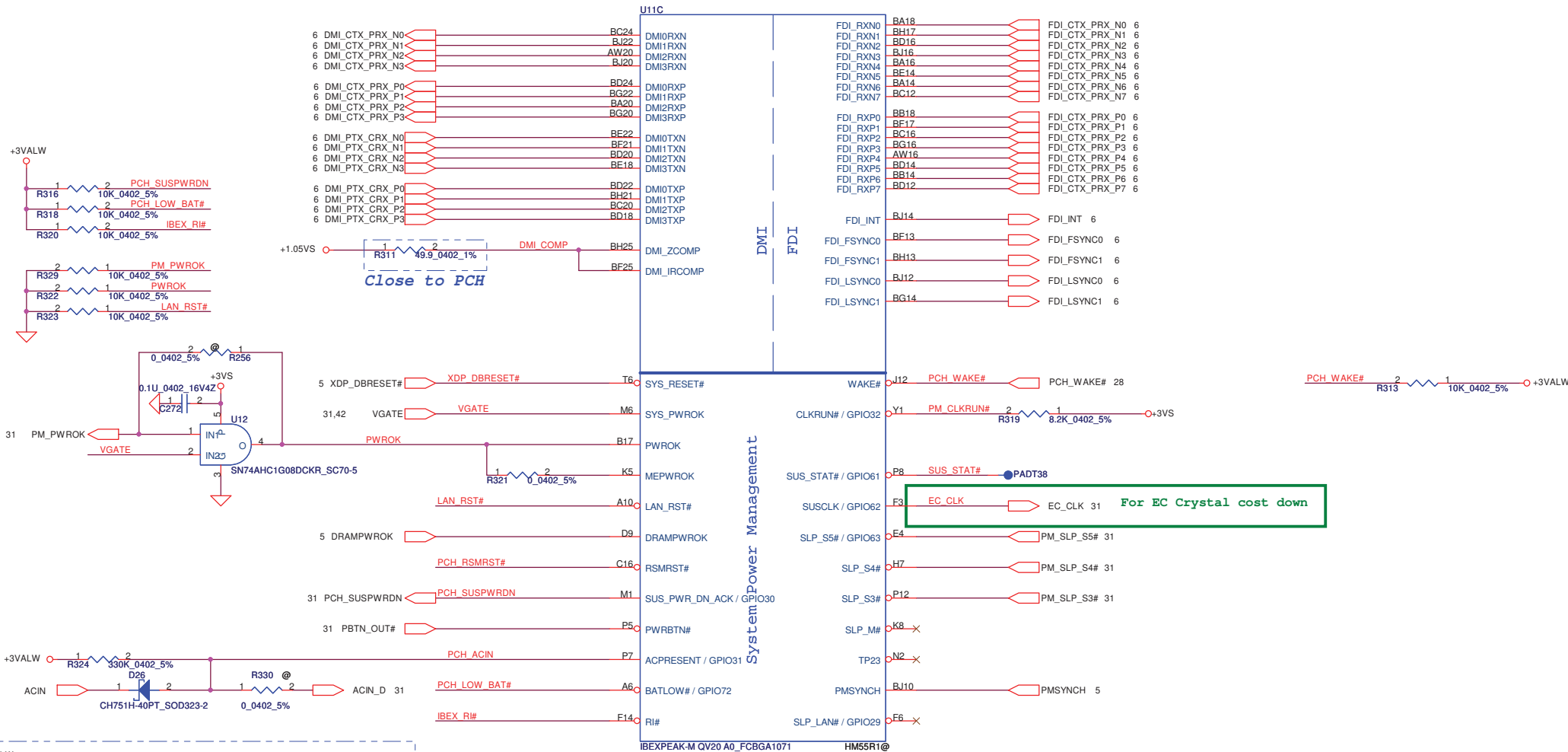


Note: Stuff 0 ohm if 25MHz crystal un-stuff

for EMI request



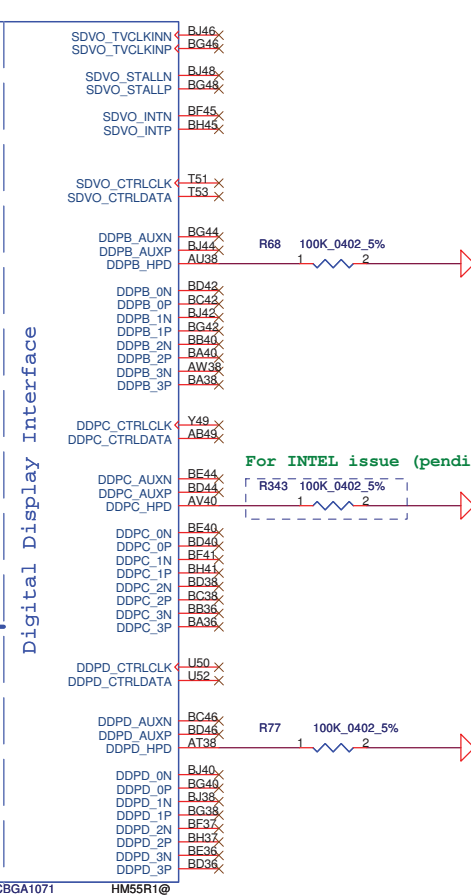
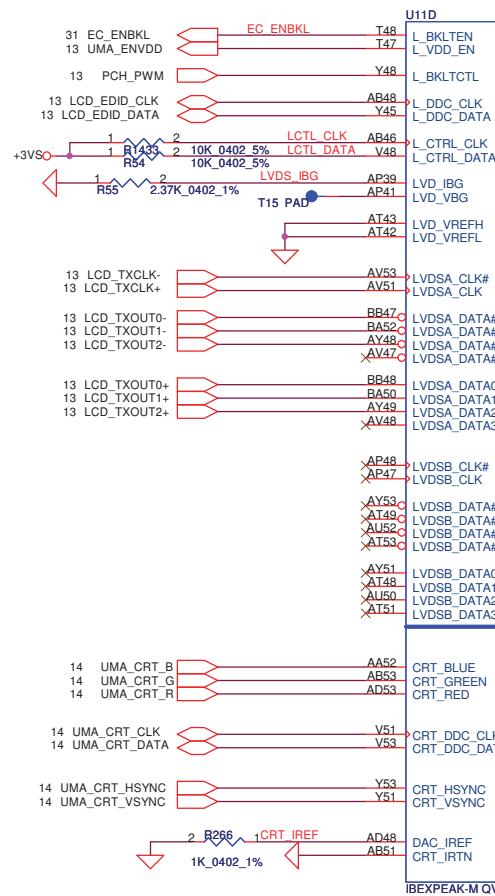
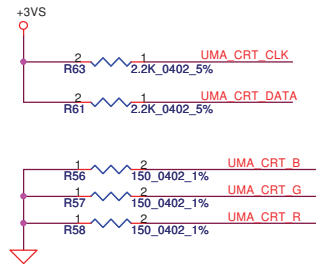
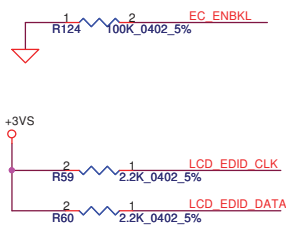
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0716 --> Unmount : R327, Q26, D15A, D15B, R328, R690
Mount : R325, D29, D28

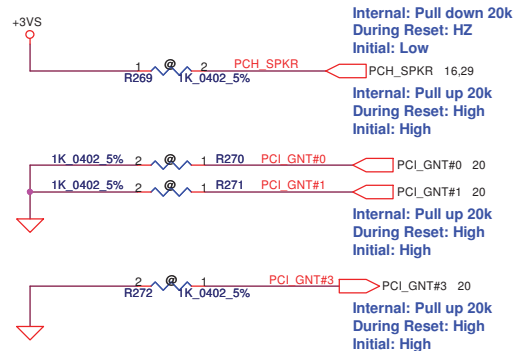
for abnormal shutdown from s3 resume

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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2010/06/21				2011/06/21				Title			
								PCH-DMI/FDI/PWM			
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								Document Number			
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								Date			
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For INTEL issue (pending interrupts from the PCH for unused HDMI ports)

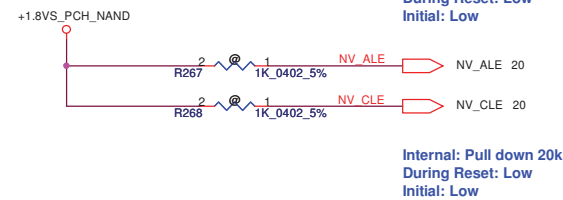
PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable
	High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled
	Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default)
	High= Set to Vcc

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				Document Number	PWWAA LA6842P M/B
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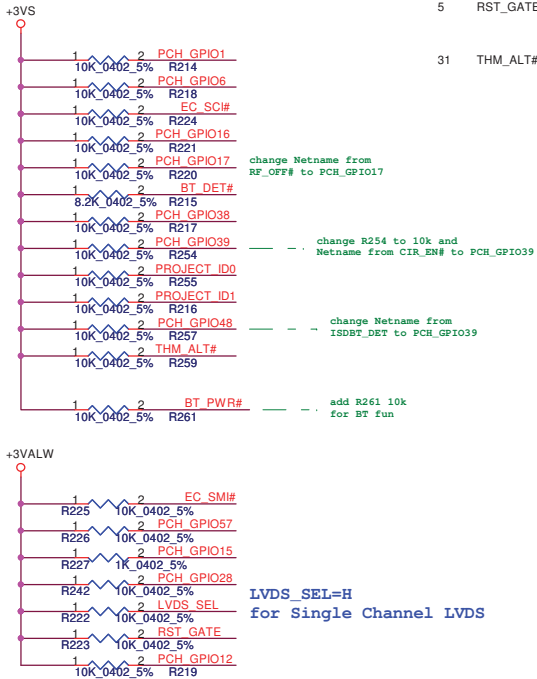
GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

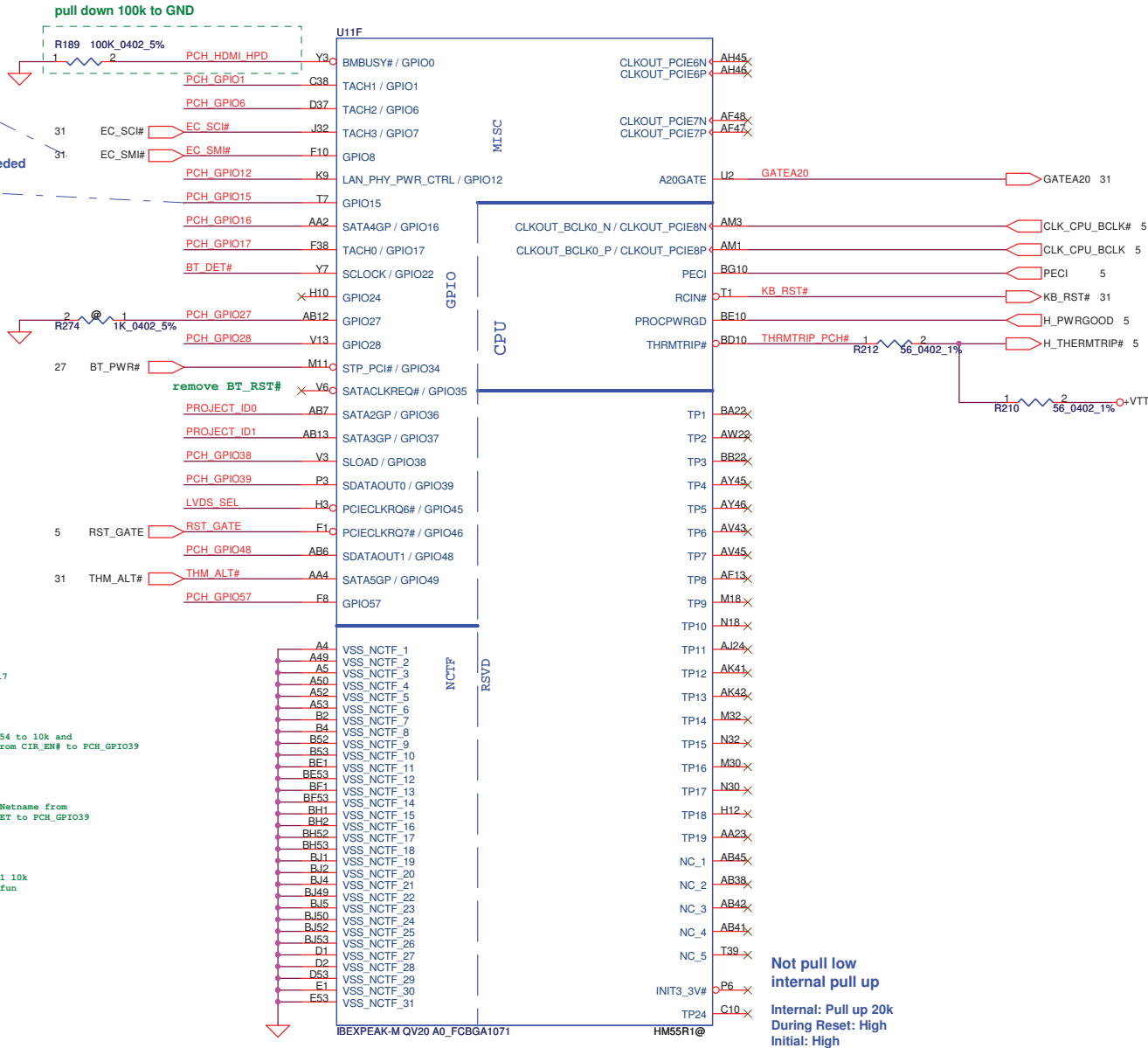
On-Die PLL VR

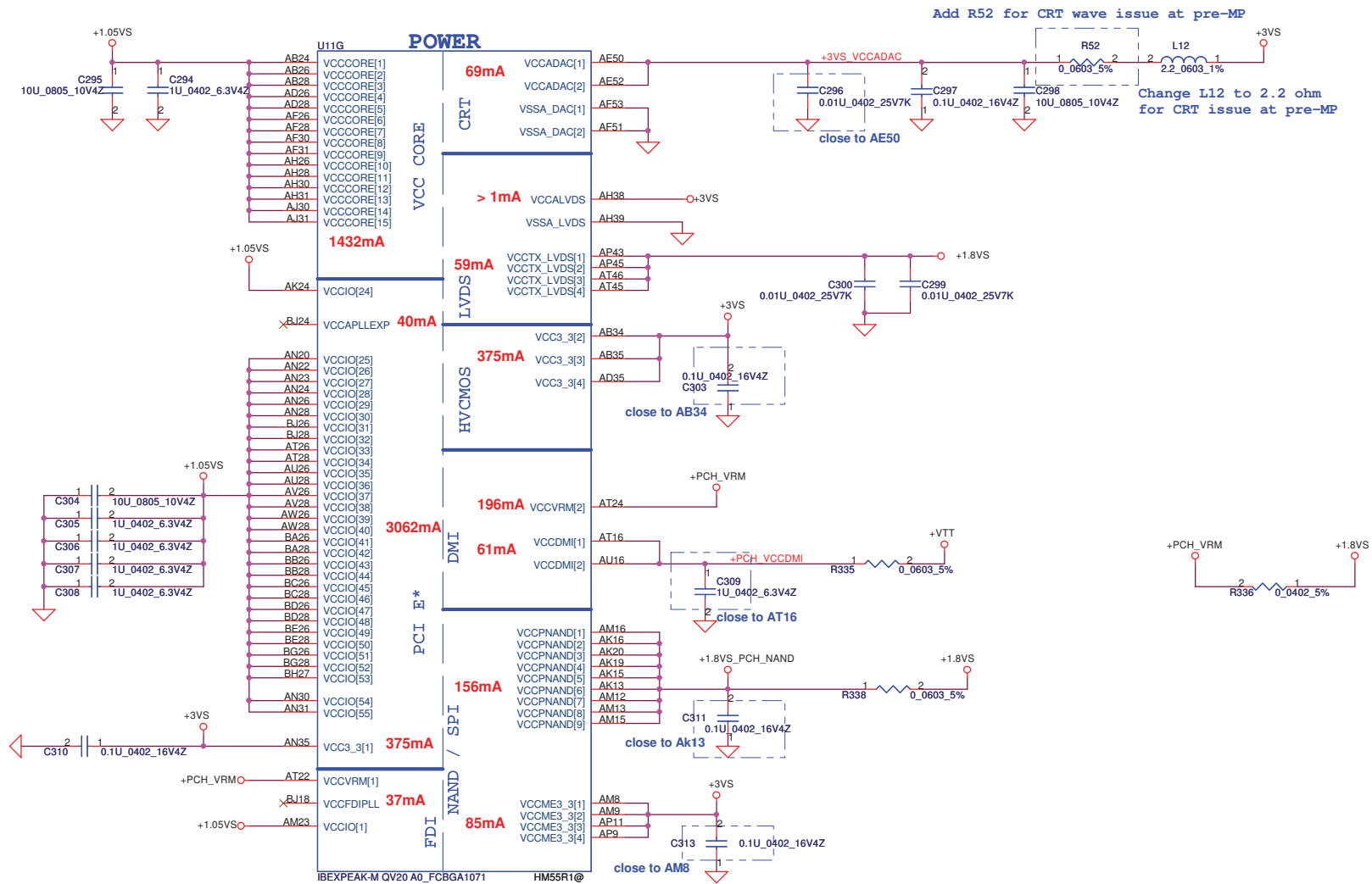
PCH_GPIO27 High = Enabled (Default)
Low = Disabled

PROJECT_ID		
Name	ID0	ID1
NBQAA 11.6/13.3"	L	L
NBQAA 14"	L	H
*NBQAA 16"	H	L
NALAA 17.3"	H	H



LVDS_SEL=H
for Single Channel LVDS





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U111		
AY7	VSS[159]	VSS[259]
B11	VSS[160]	VSS[260]
B15	VSS[161]	VSS[261]
B19	VSS[162]	VSS[262]
B23	VSS[163]	VSS[263]
B31	VSS[164]	VSS[264]
B35	VSS[165]	VSS[265]
B39	VSS[166]	VSS[266]
B43	VSS[167]	VSS[267]
B47	VSS[168]	VSS[268]
B7	VSS[169]	VSS[269]
BG12	VSS[170]	VSS[270]
BB12	VSS[171]	VSS[271]
BB16	VSS[172]	VSS[272]
BB20	VSS[173]	VSS[273]
BB24	VSS[174]	VSS[274]
BB30	VSS[175]	VSS[275]
BB34	VSS[176]	VSS[276]
BB38	VSS[177]	VSS[277]
BB42	VSS[178]	VSS[278]
BB49	VSS[179]	VSS[279]
BB5	VSS[180]	VSS[280]
BC10	VSS[181]	VSS[281]
BC14	VSS[182]	VSS[282]
BC18	VSS[183]	VSS[283]
BC2	VSS[184]	VSS[284]
BC22	VSS[185]	VSS[285]
BC32	VSS[186]	VSS[286]
BC36	VSS[187]	VSS[287]
BC40	VSS[188]	VSS[288]
BC44	VSS[189]	VSS[289]
BC52	VSS[190]	VSS[290]
BH9	VSS[191]	VSS[291]
BD48	VSS[192]	VSS[292]
BD49	VSS[193]	VSS[293]
BD5	VSS[194]	VSS[294]
BE12	VSS[195]	VSS[295]
BE16	VSS[196]	VSS[296]
BE20	VSS[197]	VSS[297]
BE24	VSS[198]	VSS[298]
BE30	VSS[199]	VSS[299]
BE34	VSS[200]	VSS[300]
BE38	VSS[201]	VSS[301]
BE42	VSS[202]	VSS[302]
BE46	VSS[203]	VSS[303]
BE48	VSS[204]	VSS[304]
BE50	VSS[205]	VSS[305]
BE6	VSS[206]	VSS[306]
BE8	VSS[207]	VSS[307]
BF3	VSS[208]	VSS[308]
BF49	VSS[209]	VSS[309]
BF51	VSS[210]	VSS[310]
BG18	VSS[211]	VSS[311]
BG24	VSS[212]	VSS[312]
BG4	VSS[213]	VSS[313]
BG50	VSS[214]	VSS[314]
BH11	VSS[215]	VSS[315]
BH15	VSS[216]	VSS[316]
BH19	VSS[217]	VSS[317]
BH23	VSS[218]	VSS[318]
BH31	VSS[219]	VSS[319]
BH35	VSS[220]	VSS[320]
BH39	VSS[221]	VSS[321]
BH43	VSS[222]	VSS[322]
BH47	VSS[223]	VSS[323]
BH7	VSS[224]	VSS[324]
C12	VSS[225]	VSS[325]
C50	VSS[226]	VSS[326]
D51	VSS[227]	VSS[327]
E12	VSS[228]	VSS[328]
E16	VSS[229]	VSS[329]
E20	VSS[230]	VSS[330]
E24	VSS[231]	VSS[331]
E30	VSS[232]	VSS[332]
E34	VSS[233]	VSS[333]
E38	VSS[234]	VSS[334]
E42	VSS[235]	VSS[335]
E46	VSS[236]	VSS[336]
E48	VSS[237]	VSS[337]
E6	VSS[238]	VSS[338]
E8	VSS[239]	VSS[339]
F49	VSS[240]	VSS[340]
F5	VSS[241]	VSS[341]
G14	VSS[242]	VSS[342]
G18	VSS[243]	VSS[343]
G2	VSS[244]	VSS[344]
G22	VSS[245]	VSS[345]
G32	VSS[246]	VSS[346]
G36	VSS[247]	VSS[347]
G40	VSS[248]	VSS[348]
G44	VSS[249]	VSS[349]
G52	VSS[250]	VSS[350]
AF39	VSS[251]	VSS[351]
H16	VSS[252]	VSS[352]
H20	VSS[253]	VSS[353]
H30	VSS[254]	VSS[354]
H34	VSS[255]	VSS[355]
H38	VSS[256]	VSS[356]
H42	VSS[257]	VSS[357]
	VSS[258]	VSS[358]

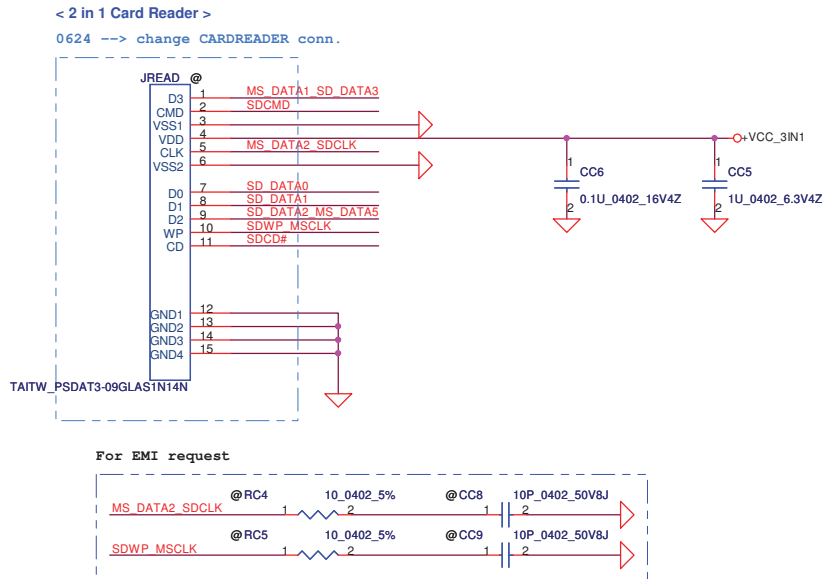
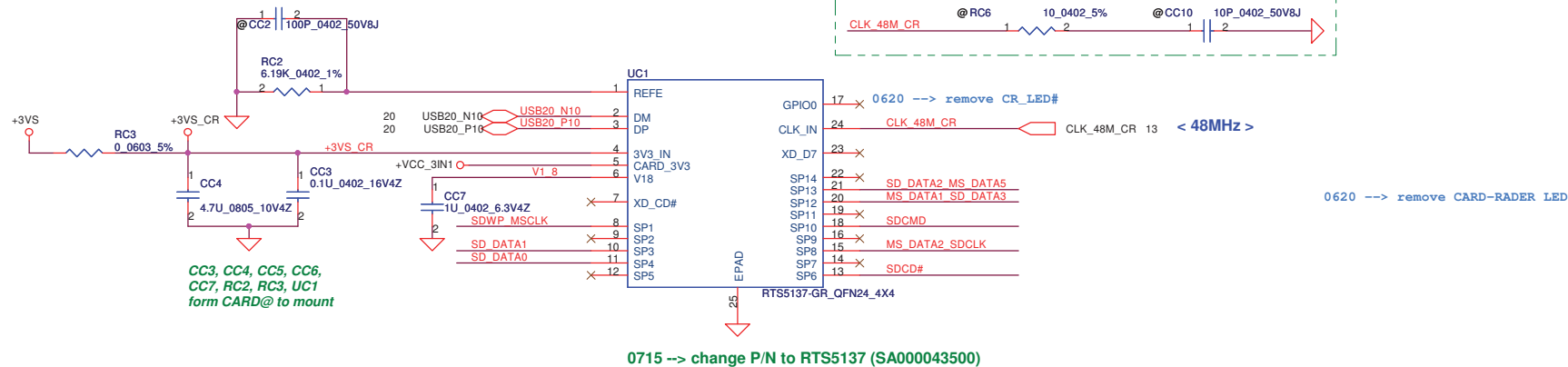
IBEXPEAK-M QV20 A0_FCBGA1071 HM55R1@

U11H		
AB16	VSS[0]	
AA19	VSS[1]	VSS[80]
AA20	VSS[2]	VSS[81]
AA22	VSS[3]	VSS[82]
AM19	VSS[4]	VSS[83]
AA24	VSS[5]	VSS[84]
AA26	VSS[6]	VSS[85]
AA28	VSS[7]	VSS[86]
AA30	VSS[8]	VSS[87]
AA31	VSS[9]	VSS[88]
AA32	VSS[10]	VSS[89]
AB11	VSS[11]	VSS[90]
AB15	VSS[12]	VSS[91]
AB23	VSS[13]	VSS[92]
AB30	VSS[14]	VSS[93]
AB31	VSS[15]	VSS[94]
AB32	VSS[16]	VSS[95]
AB39	VSS[17]	VSS[96]
AB43	VSS[18]	VSS[97]
AB47	VSS[19]	VSS[98]
AB5	VSS[20]	VSS[99]
AB5	VSS[21]	VSS[100]
AC2	VSS[22]	VSS[101]
AC52	VSS[23]	VSS[102]
AD11	VSS[24]	VSS[103]
AD12	VSS[25]	VSS[104]
AD16	VSS[26]	VSS[105]
AD23	VSS[27]	VSS[106]
AD30	VSS[28]	VSS[107]
AD31	VSS[29]	VSS[108]
AD32	VSS[30]	VSS[109]
AD34	VSS[31]	VSS[110]
AU22	VSS[32]	VSS[111]
R2	VSS[33]	VSS[112]
AD42	VSS[34]	VSS[113]
AD46	VSS[35]	VSS[114]
T12	VSS[36]	VSS[115]
AD7	VSS[37]	VSS[116]
AE2	VSS[38]	VSS[117]
AE4	VSS[39]	VSS[118]
AF12	VSS[40]	VSS[119]
Y13	VSS[41]	VSS[120]
AH49	VSS[42]	VSS[121]
AU4	VSS[43]	VSS[122]
AF35	VSS[44]	VSS[123]
AP13	VSS[45]	VSS[124]
AN34	VSS[46]	VSS[125]
AF45	VSS[47]	VSS[126]
AF46	VSS[48]	VSS[127]
AF49	VSS[49]	VSS[128]
AF5	VSS[50]	VSS[129]
AG2	VSS[51]	VSS[130]
AG52	VSS[52]	VSS[131]
AH11	VSS[53]	VSS[132]
AH15	VSS[54]	VSS[133]
AH16	VSS[55]	VSS[134]
AH24	VSS[56]	VSS[135]
AH32	VSS[57]	VSS[136]
AV18	VSS[58]	VSS[137]
AH43	VSS[59]	VSS[138]
AH47	VSS[60]	VSS[139]
AH7	VSS[61]	VSS[140]
AJ19	VSS[62]	VSS[141]
AJ2	VSS[63]	VSS[142]
AJ20	VSS[64]	VSS[143]
AJ22	VSS[65]	VSS[144]
AJ23	VSS[66]	VSS[145]
AJ25	VSS[67]	VSS[146]
AJ28	VSS[68]	VSS[147]
AJ34	VSS[69]	VSS[148]
AT5	VSS[70]	VSS[149]
AT5	VSS[71]	VSS[150]
AJ4	VSS[72]	VSS[151]
AK12	VSS[73]	VSS[152]
AM41	VSS[74]	VSS[153]
AN19	VSS[75]	VSS[154]
AK26	VSS[76]	VSS[155]
AK22	VSS[77]	VSS[156]
AK23	VSS[78]	VSS[157]
AK28	VSS[79]	VSS[158]
		VSS[80]
		VSS[81]
		VSS[82]
		VSS[83]
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		VSS[152]
		VSS[153]
		VSS[154]
		VSS[155]
		VSS[156]
		VSS[157]
		VSS[158]

IBEXPEAK-M QV20 A0_FCBGA1071 HM55R1@

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				Custom	PWWAA LA6842P M/B
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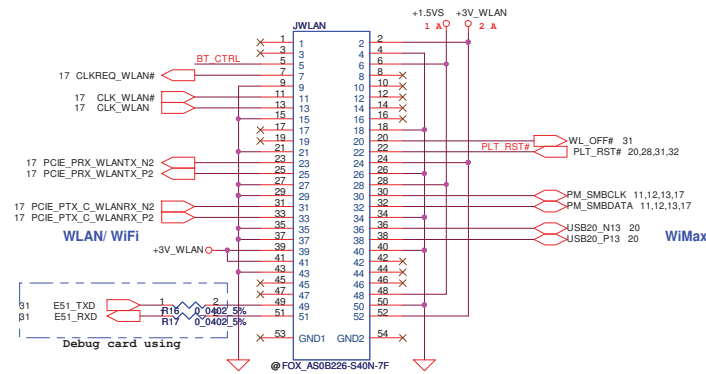
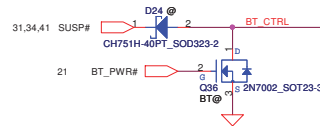
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Size		Document Number		Rev	
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Date:		Wednesday, July 28, 2010		Sheet	
		26		of 45	

PCle Mini Card-WLAN/WiMax

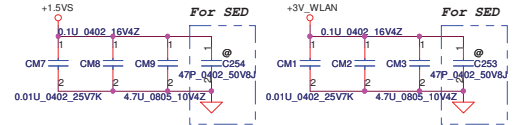
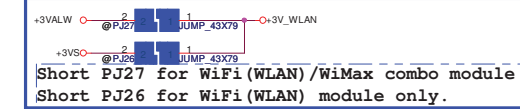
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

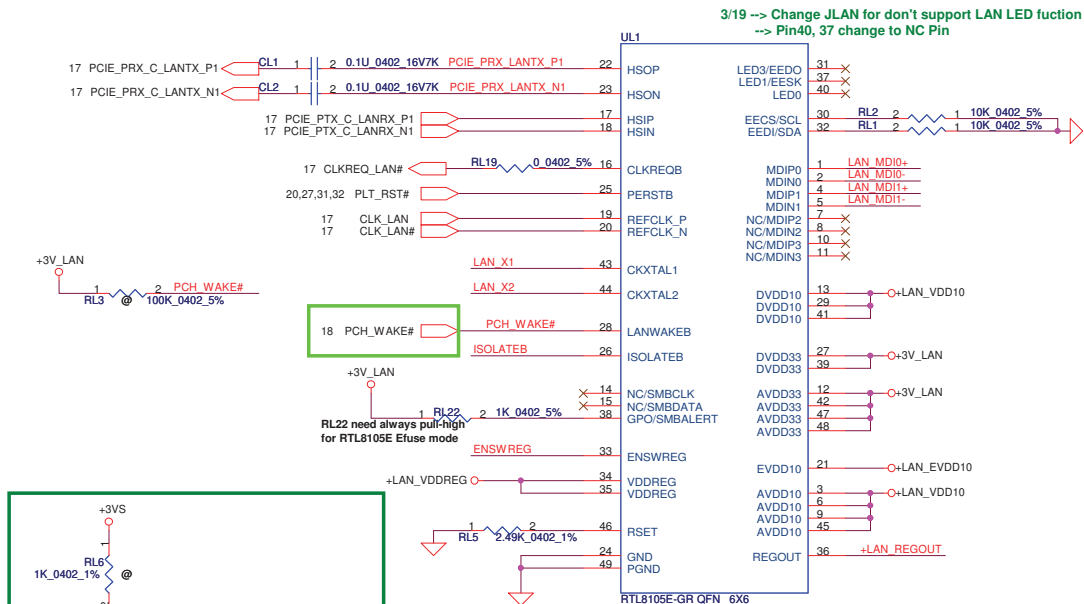
**If +3V_WLAN is +3VS, please remove D24.



Slot#1 Half PCIe Mini Card-WLAN/WiMax

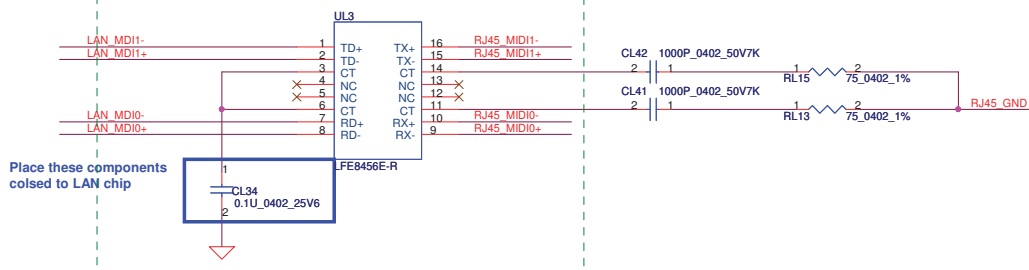


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				Size	Document Number
				Date	Wednesday, July 28, 2010
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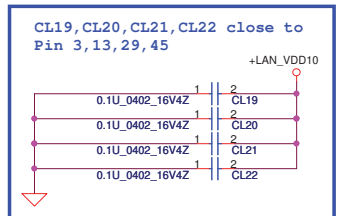
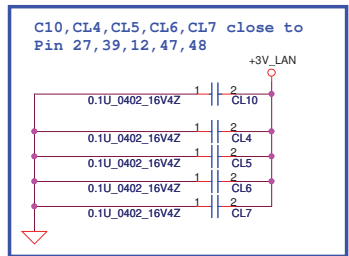
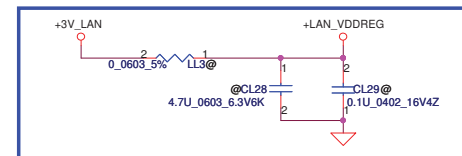
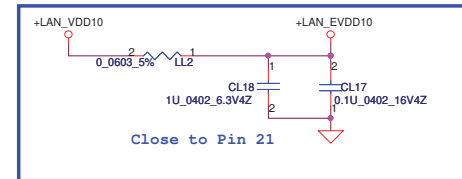
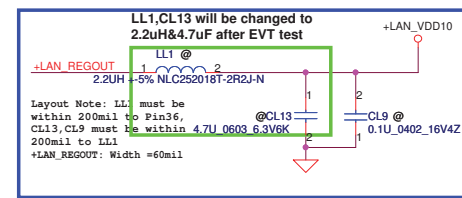


Add RL10 for +3V_LAN power enable signal
Add RL11 for wake on LAN function enable signal

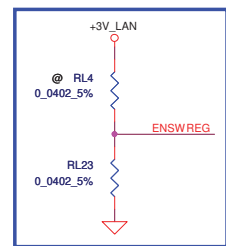
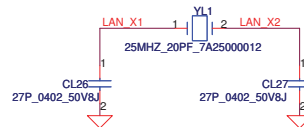
3/29 --> swap Line and PHY signal



0715 --> LL1, CL13, CL9, LL3, CL28, CL29 are unmount for RTL8105E-VC

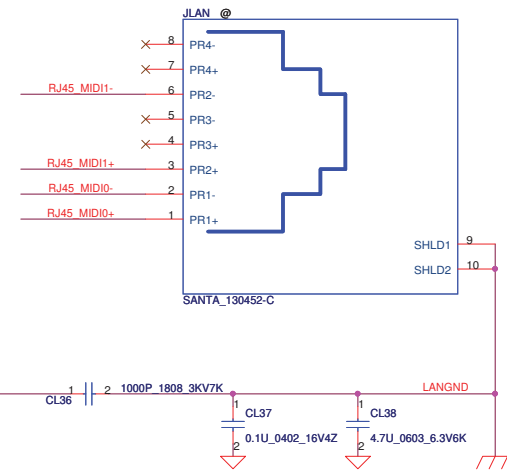


4/2-->remove RL8, RL9, CL11



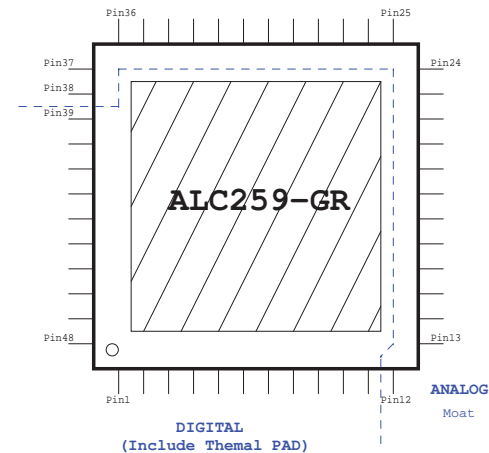
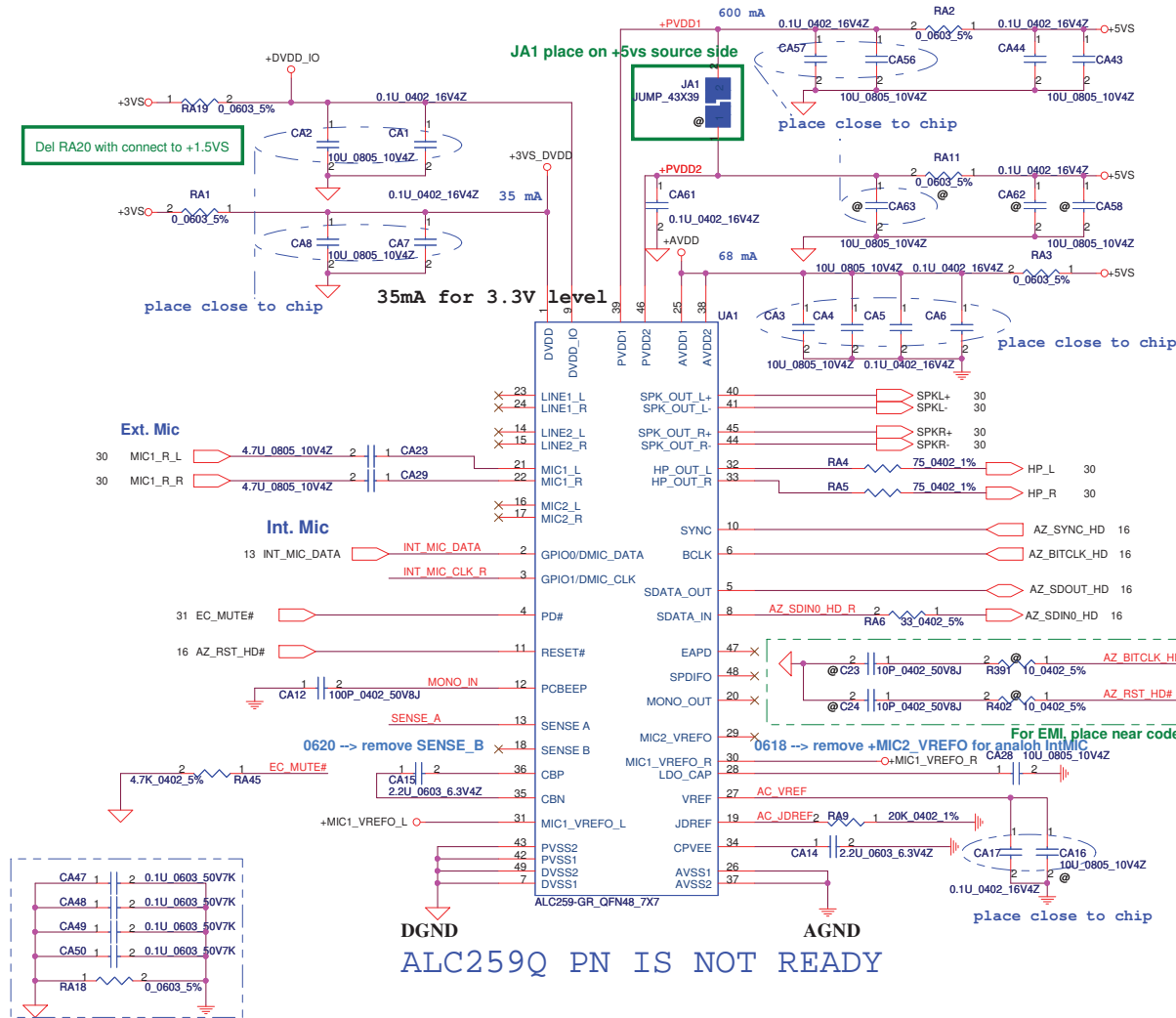
0715 --> RL4 is unmount, RL23 mount for RTL8105E-VC

LAN Conn.



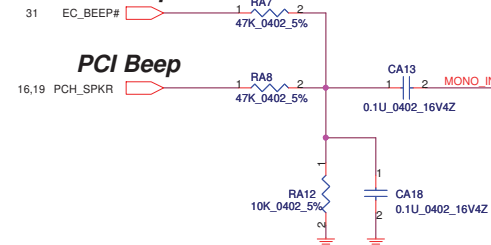
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Size Custom		Document Number		Rev	
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Codec

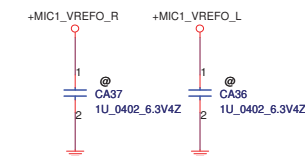


Beep sound

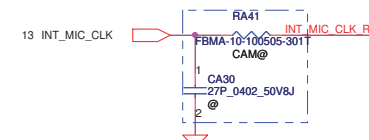
EC Beep



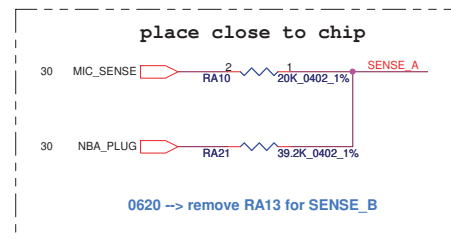
Place close to chip



For EMI

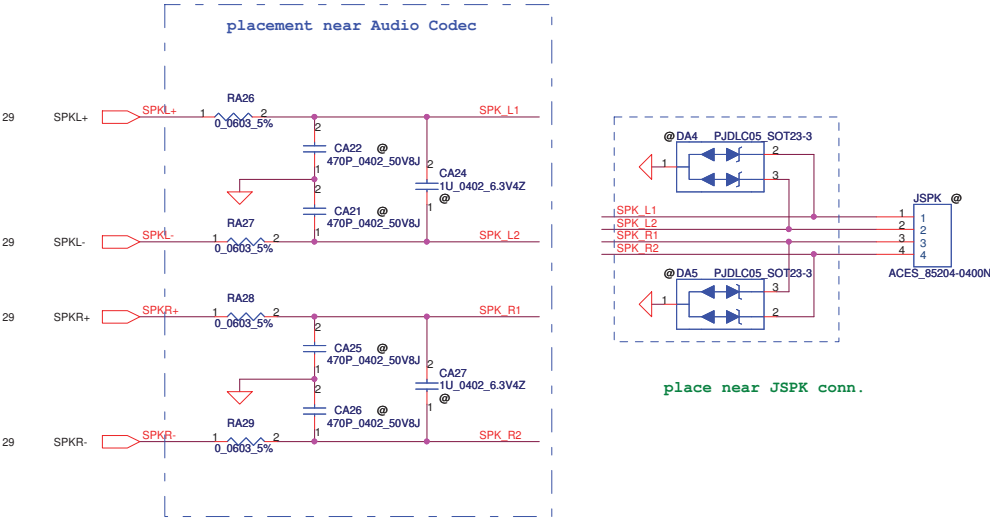


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	

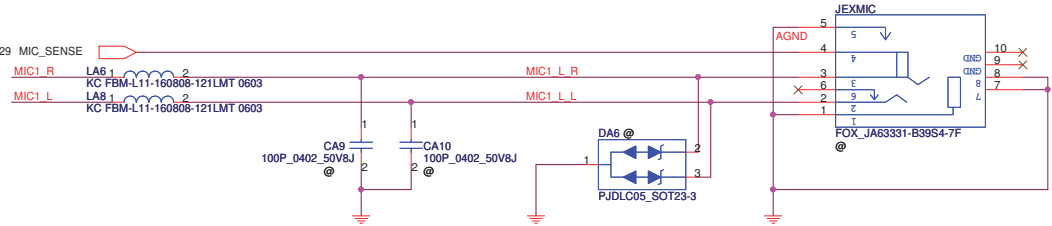


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				PWWAA	LA6842P M/B
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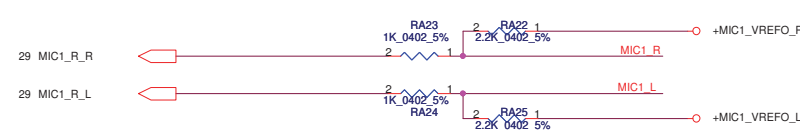
Speaker Connector



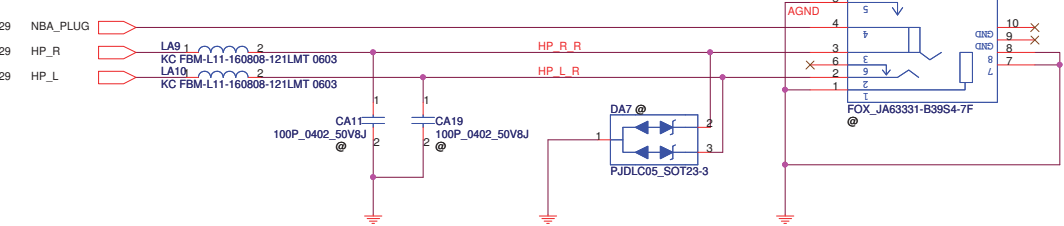
Ex.MIC JACK



Ext.MIC/LINE IN

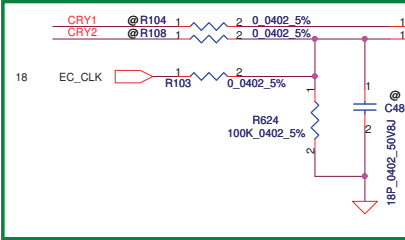
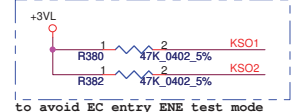
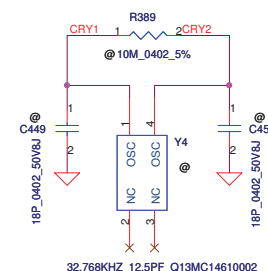
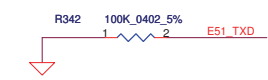
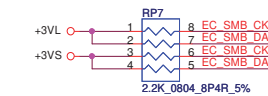
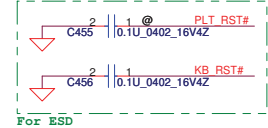
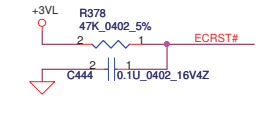
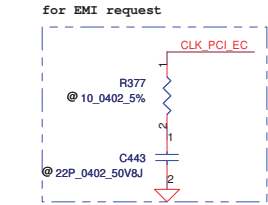


Head Phone JACK

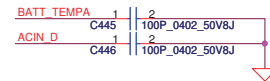
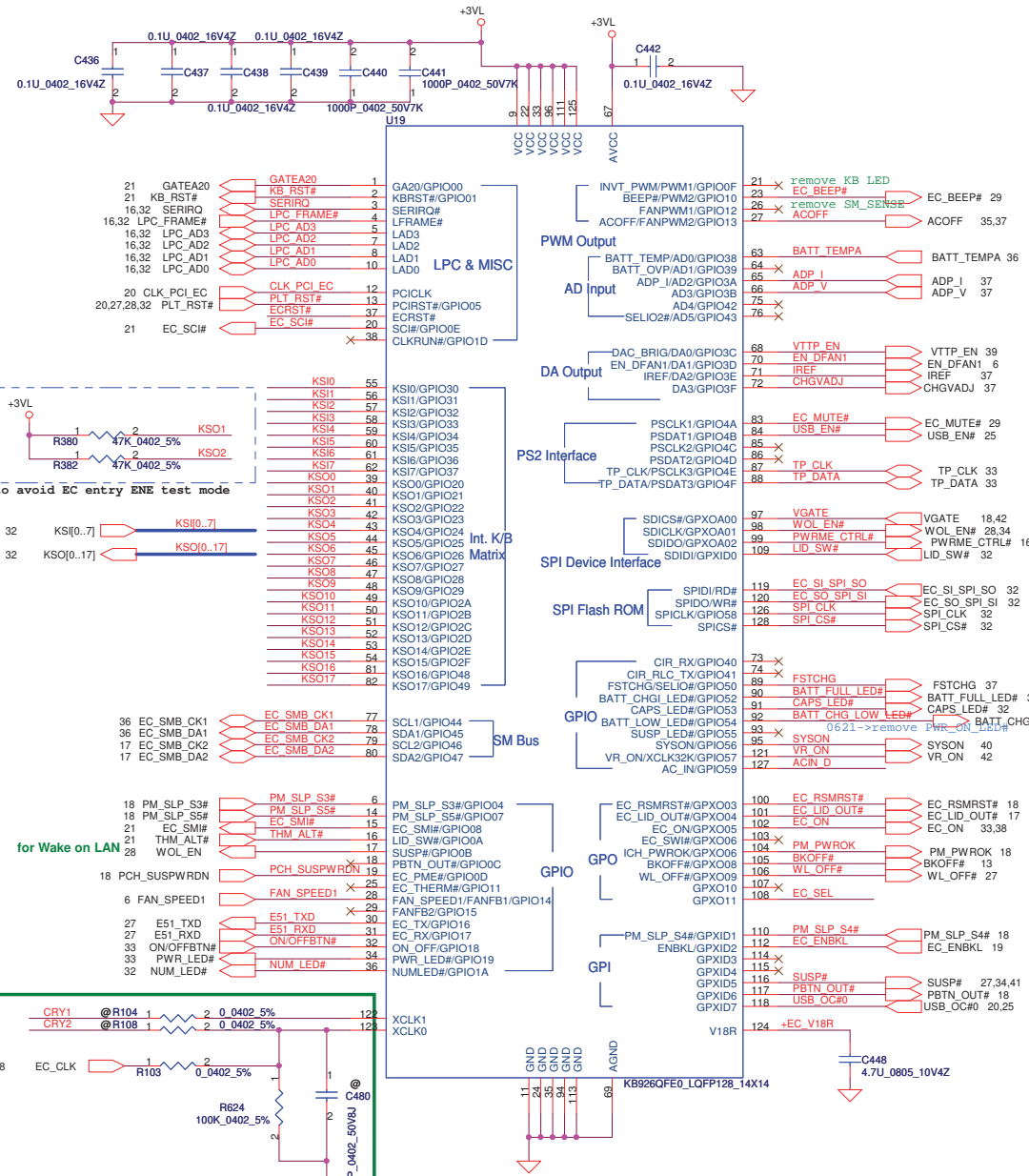


Int. Mic

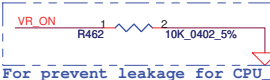
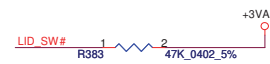
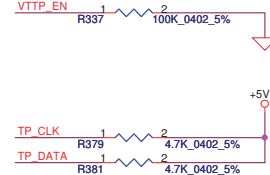
0618 --> remove Analog IntMIC, and change to DIGITAL MIC



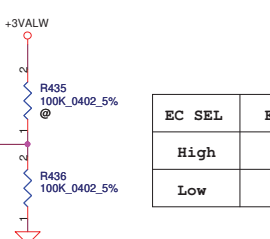
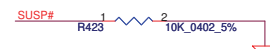
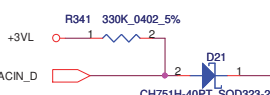
For EC Crystal cost down



Remove CEC_INT# pull high



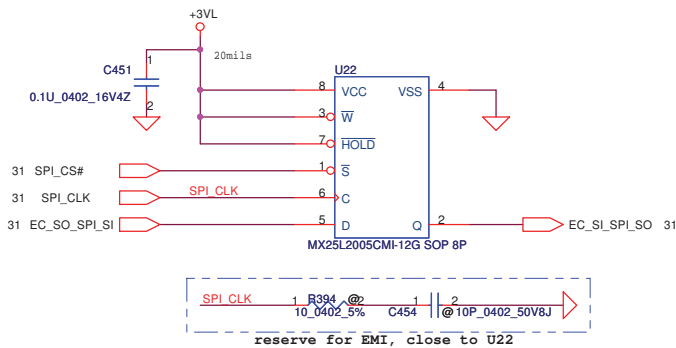
For prevent leakage for CPU_CORE



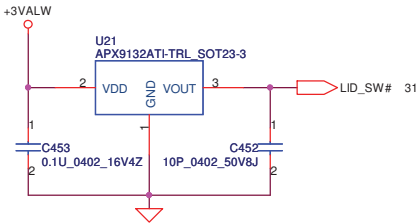
EC SEL	EC Version
High	KB926D3
Low	KB926E0

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SPI Flash (256KB)

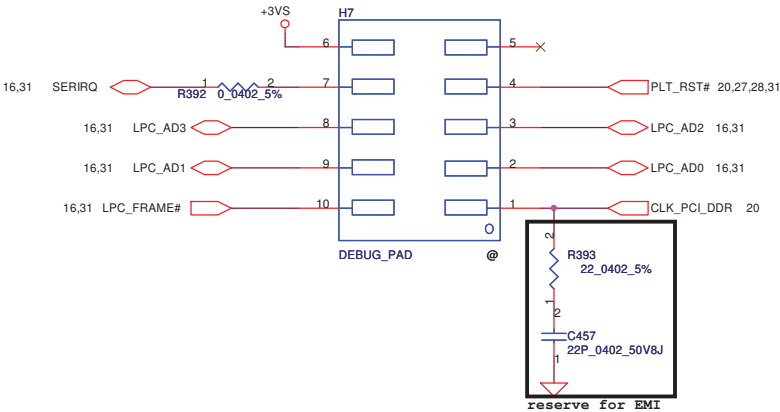


Lid SW



LPC Debug Port

Please place the PAD under DDR DIMM.

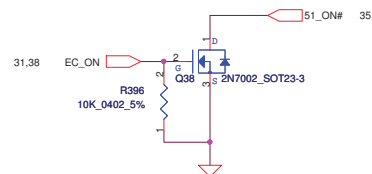
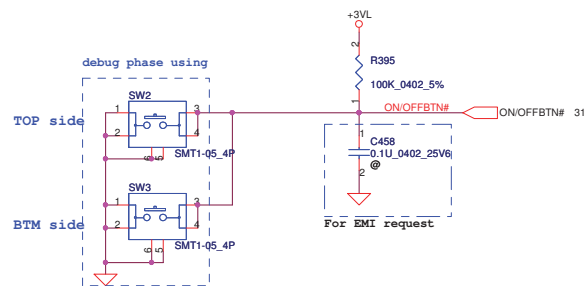


KEYBOARD CONN.

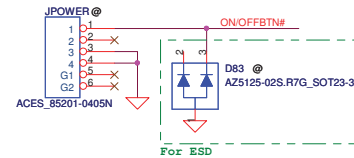


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Size		Document Number		Rev	
		PWWAA LA6842P M/B		0.2	
Date:		Wednesday, July 28, 2010		Sheet	32 of 45

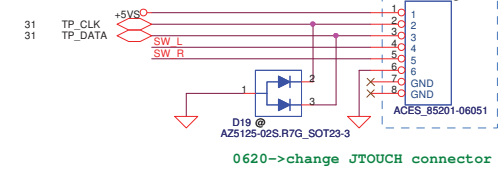
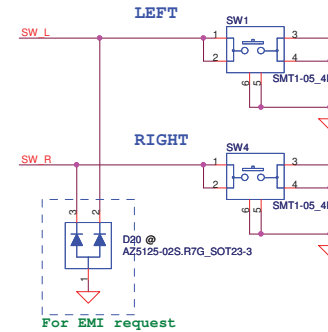
Power Button



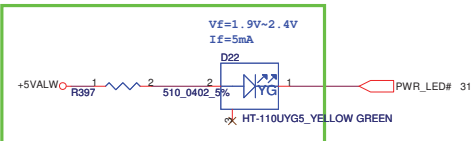
PWR/B to MB Conn.



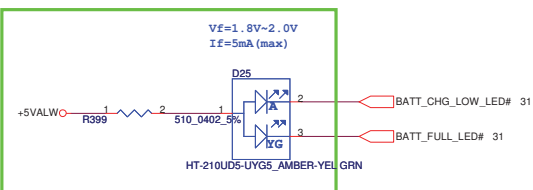
TP Button/Conn.



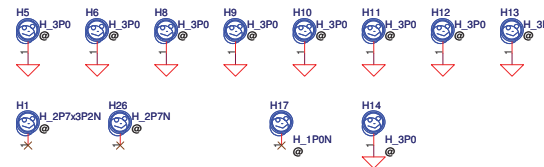
POWER/SUSPEND LED



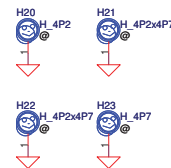
BATT CHARGE/FULL LED



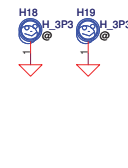
Screw Hole



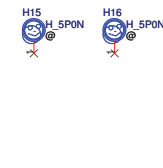
CPU



MINI CARD



SB



For Codec AGND

Dummy

3G

MDC

PCB Fedical Mark PAD



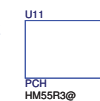
ISPD



DC-IN



PCH



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				Date:	Wednesday, July 28, 2010
				Sheet	33 of 45

[illegible][illegible][illegible]

5,39 VTTPWOK

1 2

R169 100K_0402_5%

Q48A 2N7002DW-T/R7_SOT363-6

SUSP

Q48B 2N7002DW-T/R7_SOT363-6

0.75V_EN

5

+3VALW

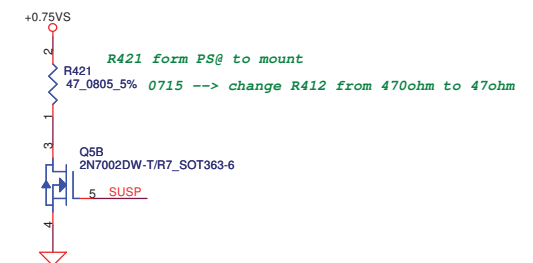
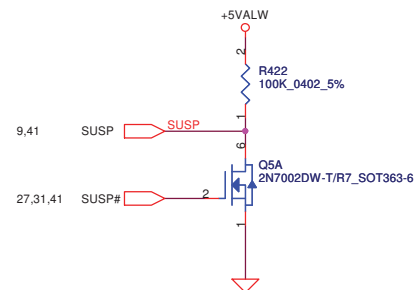
R425 100K_0402_5%

0.75V_EN# 41

Q48A,B
R169, R425 form PS@ to mount

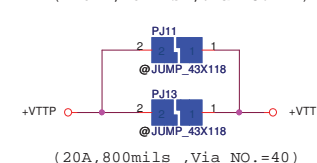
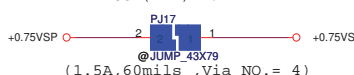
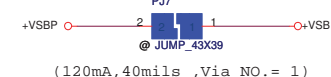
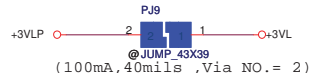
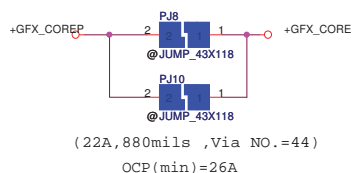
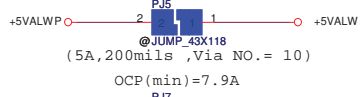
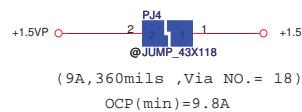
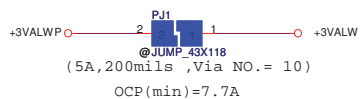
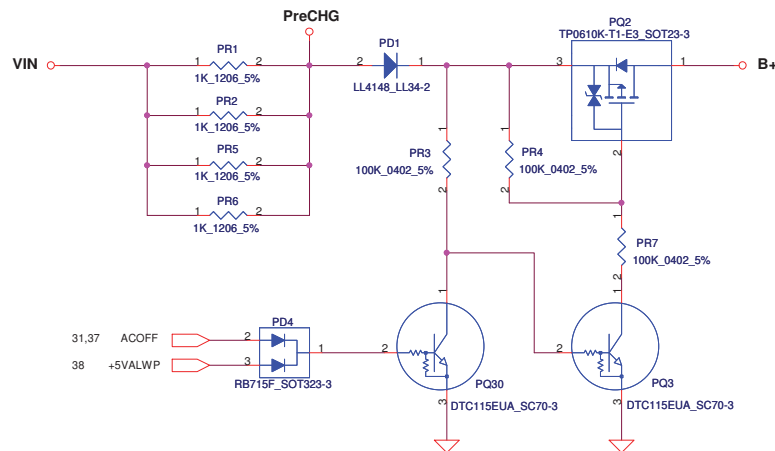
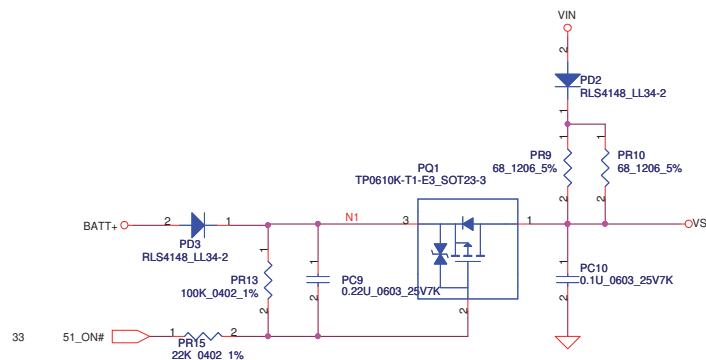
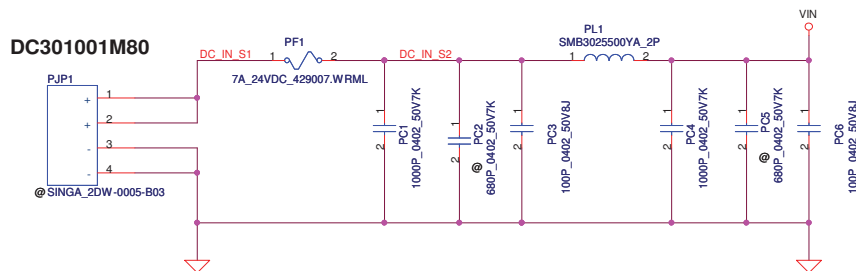
Three circuit diagrams illustrating different capacitor connections to ground:

- Diagram 1:** A capacitor labeled **C473** with value **0.1U_0402_16V7K** is connected to **+3VS** at pin 2 and to ground at pin 1.
- Diagram 2:** A capacitor labeled **C475** with value **0.1U_0402_16V7K** is connected to **+5VS** at pin 2 and to ground at pin 1.
- Diagram 3:** A capacitor labeled **C478** with value **0.1U_0402_16V7K** is connected to **+5VALW** at pin 2 and to ground at pin 1.

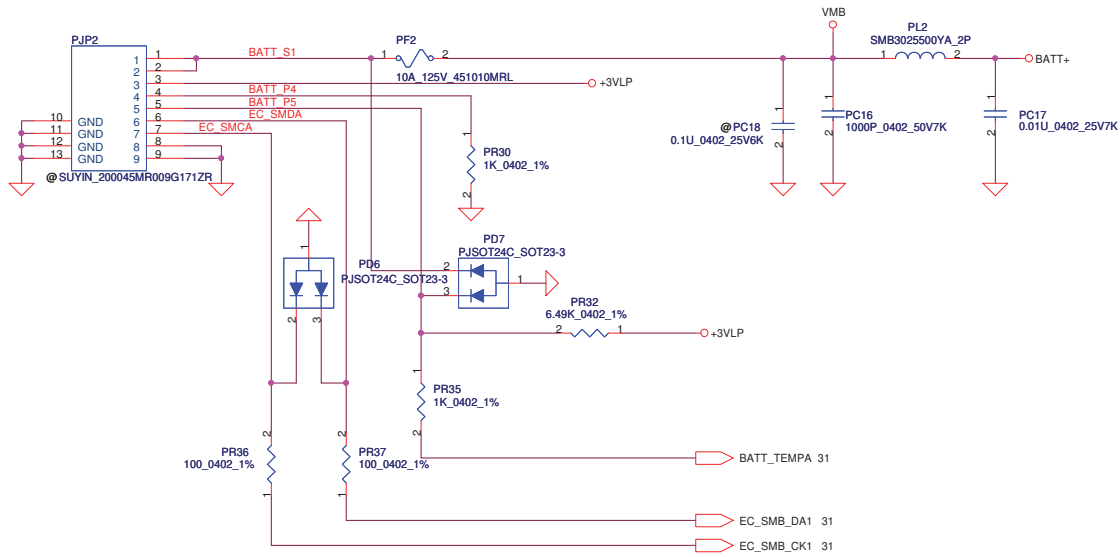


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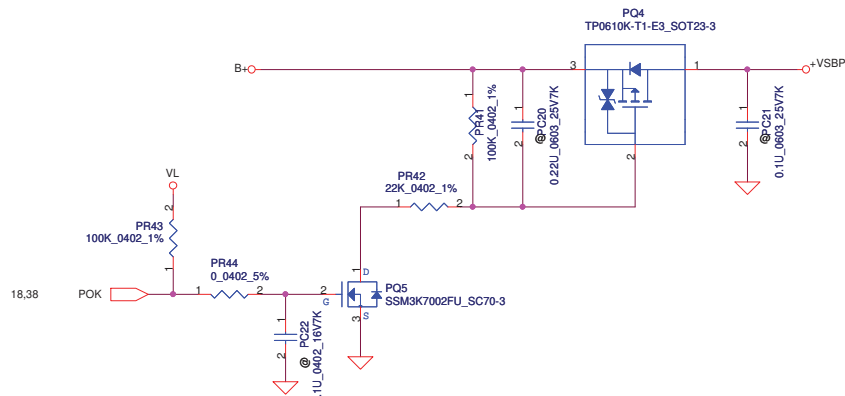
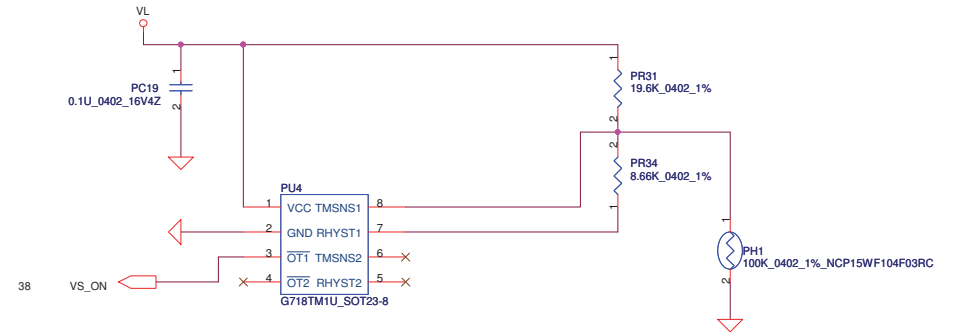
DC301001M80



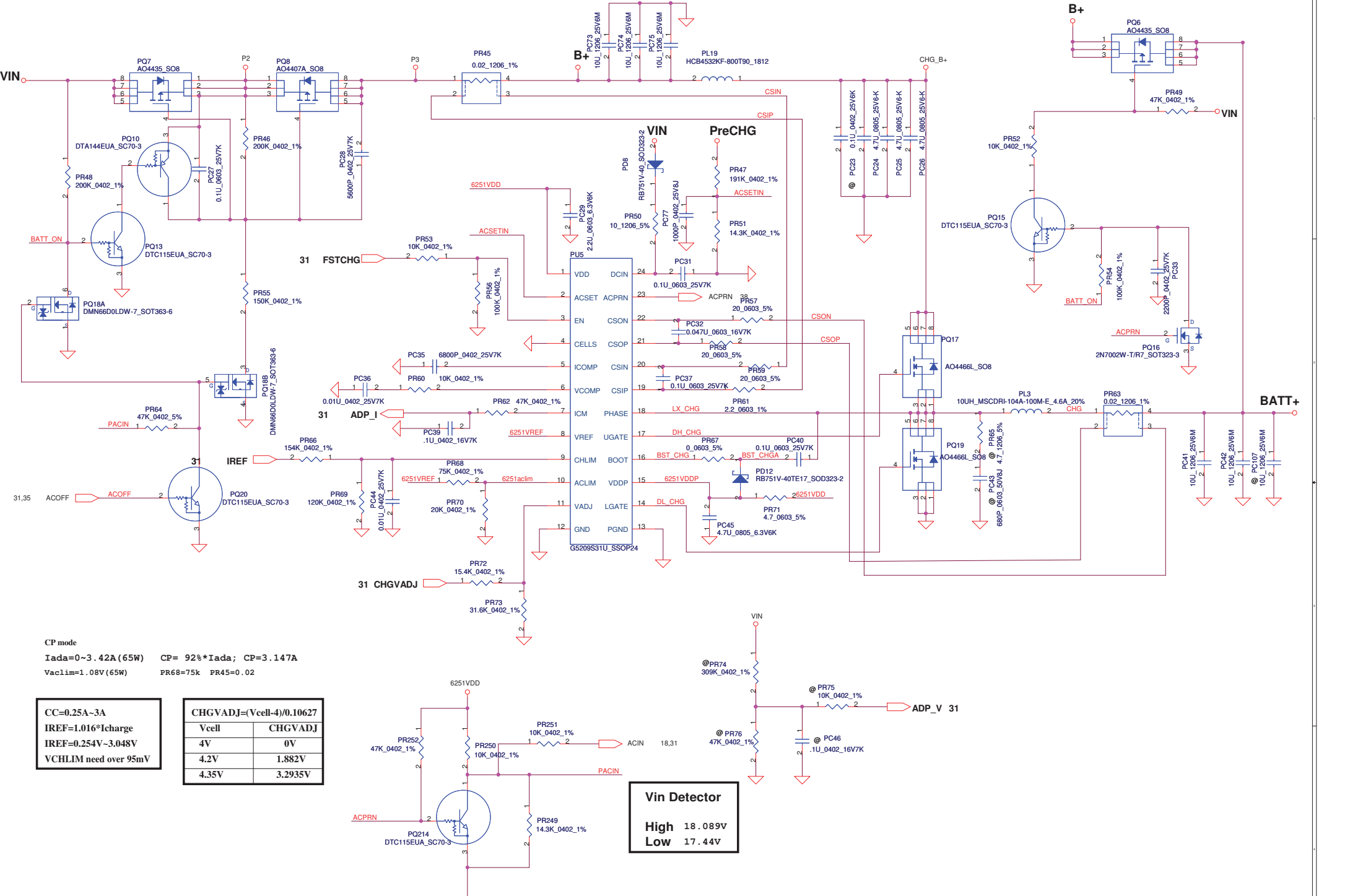
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	DCIN / DETECTOR	
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PH1 under CPU botten side :
CPU thermal protection at 95degree C
Recovery at 56 degree C



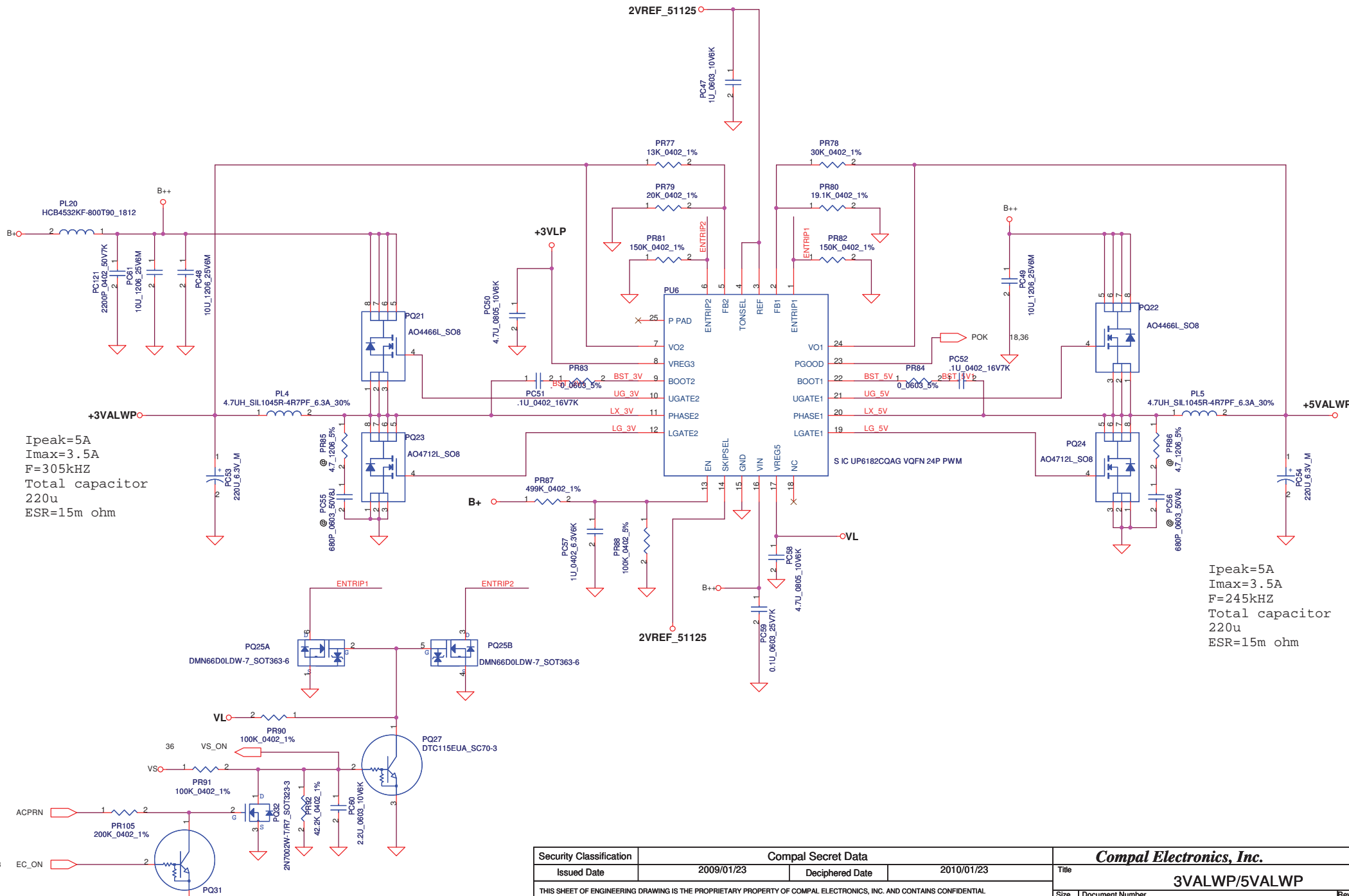
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					0.2



CP mode
 $I_{ada}=0\sim3.42A(65W)$ CP= 92%*I_{ada}; CP=3.147A
 $V_{aclim}=1.08V(65W)$ PR68=75k PR45=0.02

CC=0.25A~3A	CHGVADJ=(Vcell-4)/0.10627
IREF=1.016*Icharge	Vcell CHGVADJ
IREF=0.254V~3.048V	4V 0V
VCHLIM need over 95mV	4.2V 1.882V
	4.35V 3.2935V

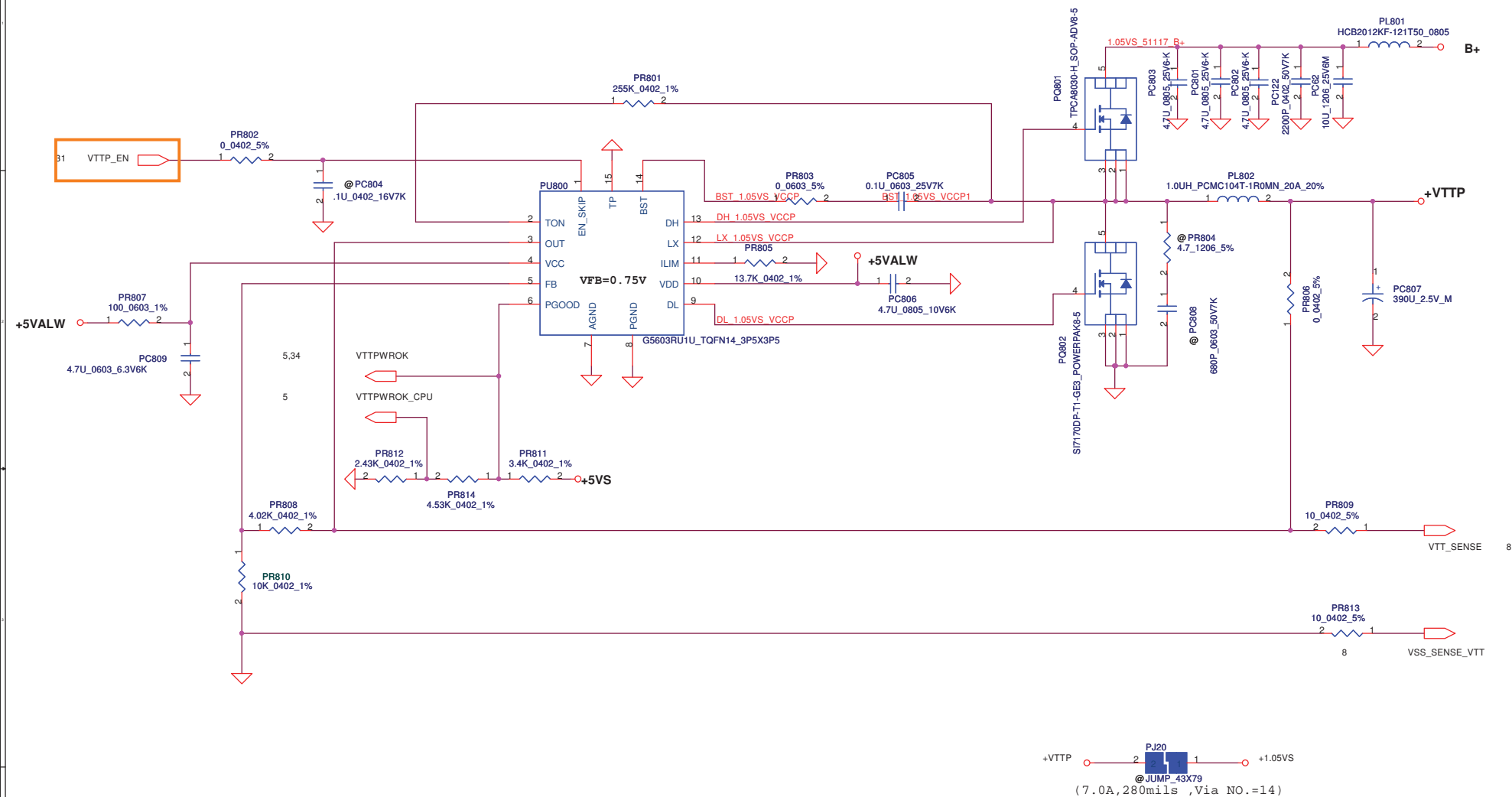
Vin Detector
High 18.089V
Low 17.44V



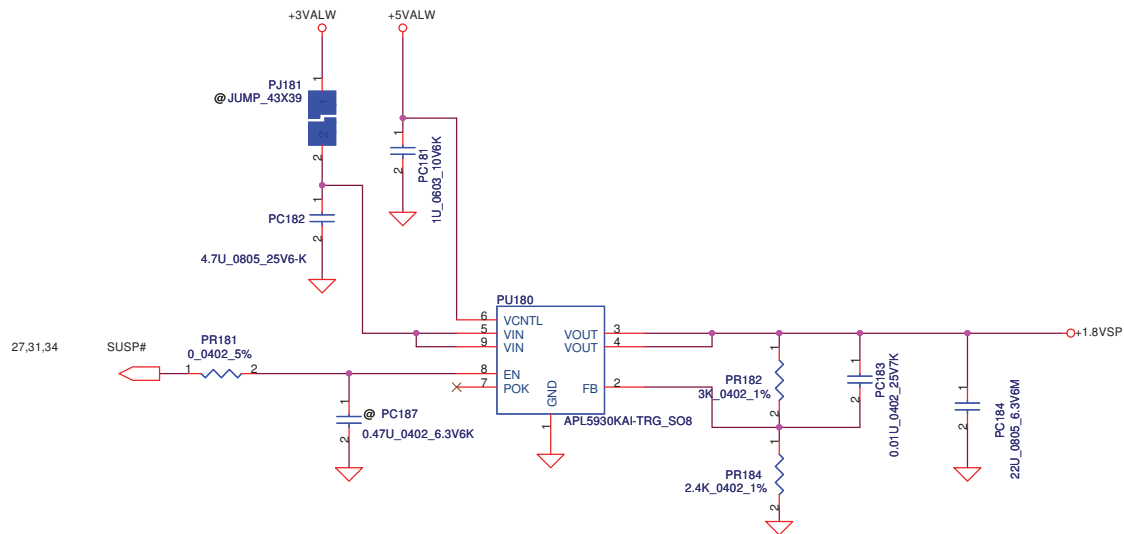
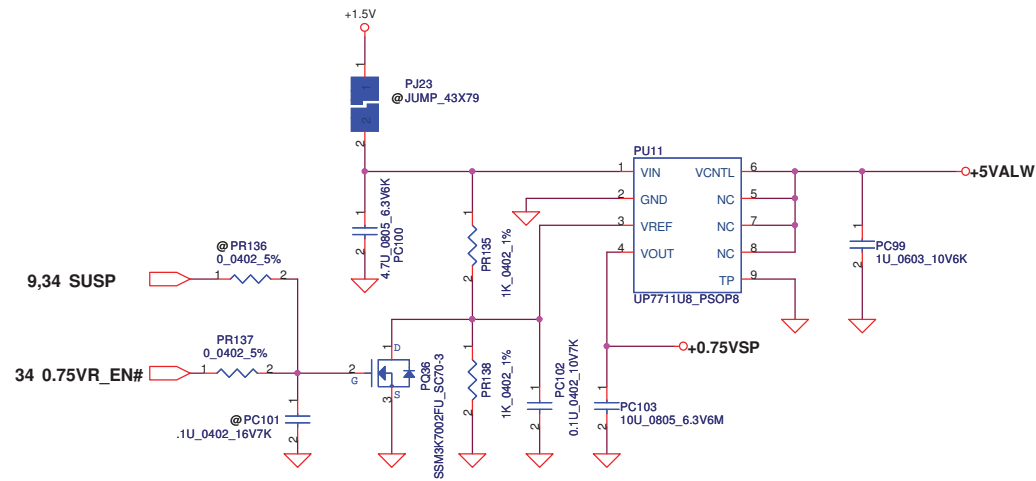
Ipeak=5A
Imax=3.5A
F=305kHz
Total capacitor
220u
ESR=15m ohm

Ipeak=5A
Imax=3.5A
F=245kHz
Total capacitor
220u
ESR=15m ohm

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Size		Document Number		PWWAA LA6842P M/B	
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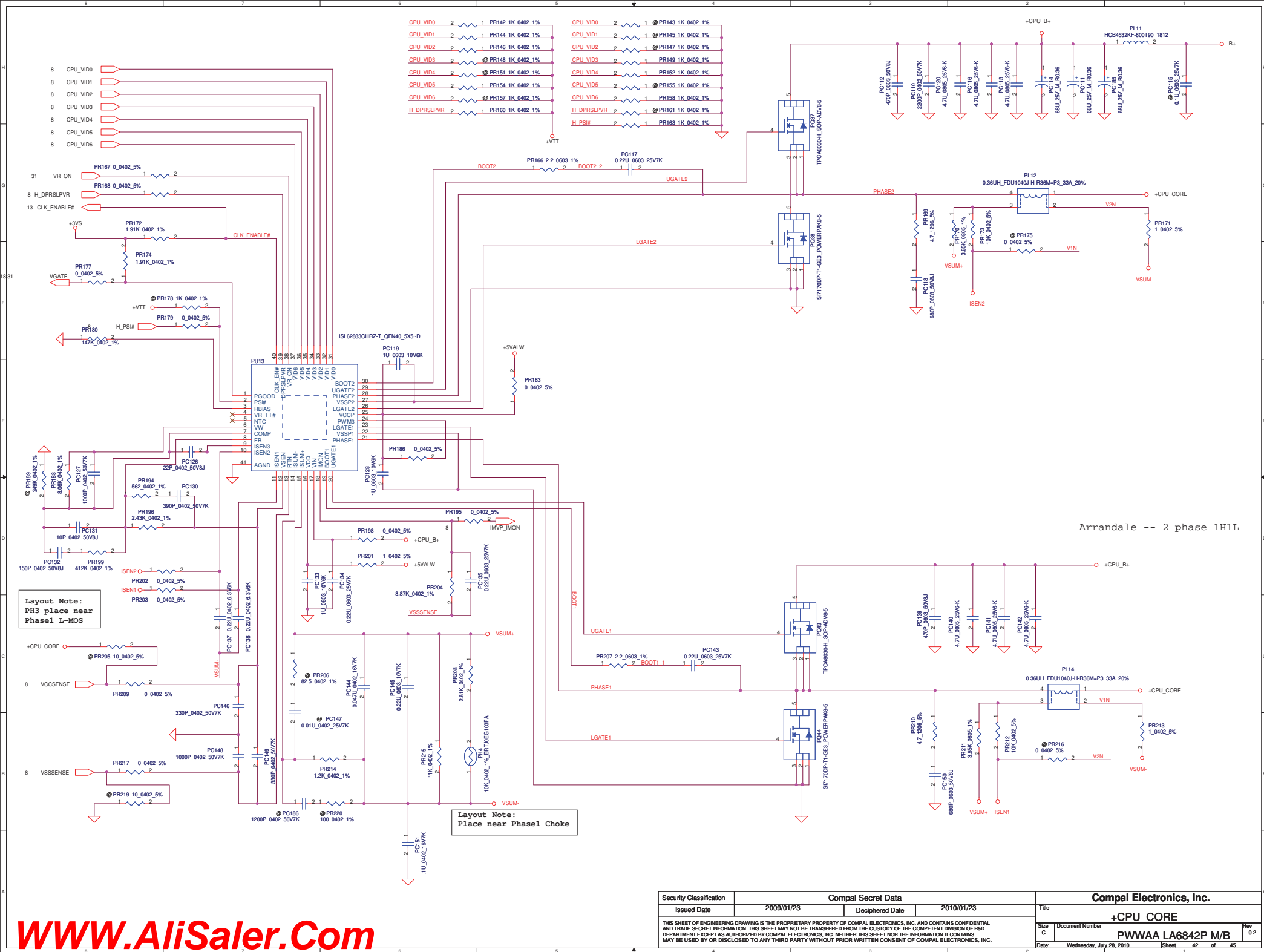


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										0.75VSP/+1.8VSP	
										PWWAA LA6842P M/B	
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/07/13	42		Change PL12,PL14 to SH00000IN00	BOM modify
2010/07/13	43		Change PL16 to SH00000IN00	BOM modify
2010/07/23	36		Change PC19 to SE070104Z80	BOM modify
2010/07/26	36		Add PD6,PD7	EMI request
2010/07/26	37		Add PC73,PC74,PC75(10U_1206)	EMI request
2010/07/26	38		Add PC121(2200P_0402),PC61(10U_1206)	EMI request
2010/07/26	39		Add PC122(2200P_0402),PC62(10U_1206)	EMI request
2010/07/26	40		Add PC123(2200P_0402)	EMI request

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PIR (Product Improve Record)

PWWAA LA-6842P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2010/07/31
NO DATE PAGE MODIFICATION LIST

PURPOSE

1. 20100714 / Page13 --> add 10u Cap to +1.5VS_CK505 For eSATA transmit issue ---> not add 10u Cap into schematic yet

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0 TO 2.0
GERBER-OUT DATE: 2010/03/19
NO DATE PAGE MODIFICATION LIST

PURPOSE

1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue